

with a marked-up copy of the substitute specification filed on August 20, 2001, for the Examiner's convenience. Applicants submit that the replacement substitute specification includes no new matter. Therefore, entry of the Substitute Specification is respectfully requested.

Claim 10 has been amended to correct the dependency thereof and the abstract has also been amended to correct errors of a grammatical nature. A copy of the marked up claim 10 and abstract is enclosed.

Entry of the preliminary amendments and examination of the application is respectfully requested.

To the extent necessary, applicant's petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (503.39864X00) and please credit any excess fees to such deposit account.

Respectfully submitted,



Melvin Kraus  
Registration No. 22,466  
ANTONELLI, TERRY, STOUT & KRAUS, LLP

MK/DRA/cee  
Attachments  
(703) 312-6600



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SUBSTITUTE SPECIFICATION

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

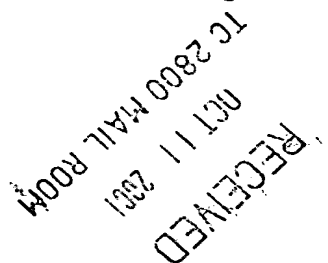
[0001]

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device  
5 and to a method of [manufacturing] method of manufacture  
thereof; and, more particularly, the invention relates to a  
semiconductor device [and a manufacturing method thereof that]  
in which a semiconductor element has at least a stress  
cushioning layer and a semiconductor protective layer, and the  
10 end faces of these layers are positioned inside the cutting  
scribe lines formed on a semiconductor wafer, and the range of  
the surface at the end of the semiconductor element from the  
end face to the inside of the scribe line is exposed.

[0002]

15 Recently, there [are] has been an increasing [requests]  
demand for miniaturization and high performance in various  
electronic elements; and, in association with [those] this  
demand, there have also been requests[, also] for a  
semiconductor device using electronic elements[, capable of  
20 speeding up [of] information processing, as well as high  
density packing and high density assembly [are required] of  
the electron elements. Namely, in correspondence with these  
requests, there have been changes in the general character of  
a semiconductor device [is moving] from the pin insertion type  
25 to the surface mounting type so as to increase the mounting



density; and order to [correspond to] provide a multi-pin configuration, various packages from a DIP (dual inline package) to a QFP (quad flat package) or a PGA (pin grid array) have been developed.

5 [0003]

However, in the QFP type package, the connection lead wires for connecting with the mounting substrate are centralized in the peripheral part of the package and the connection lead wires themselves are thin and deformable, so  
10 that, as the number of pins increases, the mounting [is getting hard] becomes more difficult. In the PGA type package, the terminals to be connected to the mounting substrate are thin and long and a considerable number of terminals are centralized, so that high speed processing of  
15 information is difficult from the viewpoint of characteristics; and, moreover, the PGA arrangement is of a pin insertion type, so that surface mounting is not available, and it is disadvantageous in a high density assembly.

[0004]

20 Recently, to solve various problems [of] concerning these packages and to realize a semiconductor [corresponding to] capable of high speed processing of information, a BGA (ball grid array) package having a stress cushioning layer between the semiconductor element and the substrate [with] on which a  
25 wiring circuit is formed and a bump electrode which is an external terminal on the mounting substrate surface side of the substrate with the wiring circuit [formed] has been

developed, and the [contents] details thereof are disclosed in the specification of USP 5148265. In the package described in the specification of USP 5148265, since the terminals to be connected to the mounting substrate are ball-shaped solder  
5 terminals, the lead wires are free of deformation, unlike the QFP type; and, since the terminals are scattered [overall] over the entire mounting surface, the pitch between the terminals is large and surface mounting can be [carries] carried out easily. The bump electrode which is an external  
10 terminal is shorter in length than that of the PGA type, so that the inductance component is decreased, and the information processing speed is increased, and high speed processing of information is made possible.

[0005]

15 On the other hand, recently, in association with wide spread use of portable information terminals, there [are] is an increasing [requests] demand for miniaturization and high density assembly of a semiconductor device. Therefore, recently, a CSP (chip scale package) [that the] having a  
20 package size that is almost equal to the chip size has been developed, and, for example, various types of CSPs are disclosed in "Nikkei Microelement" (pp. 38-64) issued by Nikkei BP, Ltd. (February 1998). CSPs disclosed in [it] this publication are manufactured in such a way that semiconductor  
25 elements cut into pieces are bonded onto a polyimide or ceramics substrate [with] on which a wiring layer is formed, and then the wiring layer and semiconductor elements are

electrically connected, [by a means] such as by wire bonding, single point bonding, gang bonding, or bump bonding, and the connections are sealed with resin, [and finally] after which external terminals such as solder bumps are formed thereon.

5 [0006]

In Japanese Patent Application Laid-Open 9-232256 and Japanese Patent Application Laid-Open 10-27827, methods for mass-producing CSPs are disclosed. [The] These manufacturing methods form bumps on a semiconductor wafer, electrically  
10 connect a wiring substrate via the bumps, [seals] seal the connections with resin, [forms] form external electrodes on the wiring substrate, and finally [cuts] cut the semiconductor wafer into pieces, thus [manufactures] producing individual semiconductor [devicees] devices. Furthermore, "Nikkei  
15 Microelement" (p. 164 to p. 167) issued by Nikkei BP, Ltd. (April 1998) discloses another manufacturing method for mass-producing CSPs. This manufacturing method forms bumps by plating on a semiconductor wafer, seals the part other than the bumps with resin, forms external electrodes in the bumps,  
20 then cuts the semiconductor wafer into pieces, [and manufactures] thus producing individual semiconductor [devicees] devices. In addition [to it], Japanese Patent Application Laid-Open 10-92865 discloses a semiconductor device of a type [that] in which a resin layer for cushioning  
25 stress is installed between external electrodes and semiconductor elements. Individual semiconductor [devicees] devices are manufactured by processing [in] units of

semiconductor wafers in a batch and finally cutting each semiconductor wafer into pieces.

[0007]

The aforementioned semiconductor [devicees] devices (semiconductor package) of [a] the type [that] in which a plurality of resin layers and external electrodes are formed in units of semiconductor wafers in a batch, and then each semiconductor wafer is cut (diced) into pieces, [thereby individual semiconductor devices are manufactured] has a constitution such that the interfaces of a plurality of resin layers sequentially formed on each semiconductor wafer are exposed on the end face of each semiconductor package, so that when a large mechanical stress is applied to the interfaces of the plurality of resin layers at the time of dicing of the semiconductor wafer, or when a large thermal stress is applied to the interfaces of the plurality of resin layers due to sudden temperature changes at the time of mounting of the semiconductor package, the stress is centralized to the interfaces between the semiconductor element exposed on the end face of the semiconductor package and the plurality of resin layers, [thus] so that one or more of the plurality of resin layers are peeled off and the semiconductor package may be damaged.

[0008]

As mentioned above, such a known semiconductor device cannot always [obtain] exhibit high reliability, and it is difficult to obtain a high [manufacture] manufacturing yield

rate.

[0009]

The present invention was developed [with] in view of the foregoing technical background [in view] and is intended to provide a semiconductor device, and a [manufacturing] method of manufacture thereof, having high reliability and a satisfactory manufacturing yield rate, such that the constituent part to which a concentrated stress is applied at the time of cutting of a semiconductor wafer and at the time of mounting of a semiconductor device is improved so as to withstand the stress [and], whereby the occurrences of damage of the semiconductor [devicees] devices due to applied stress are greatly reduced.

[0010]

To accomplish the above object, the semiconductor device of the present invention has semiconductor elements obtained by cutting a semiconductor wafer, having an integrated circuit and an electrode pad formed on one side thereof, along [the] a cutting scribe line[,]; a stress cushioning layer installed on the semiconductor elements[,]; a lead wire portion extending from the electrode pad to the top of the stress cushioning layer through an opening formed in the stress cushioning layer on the electrode pad[,]; external electrodes arranged on the lead wire portion on the top of the stress cushioning layer[,]; and a conductor protective layer installed on the stress cushioning layer, excluding the external electrode arranged portion; and a conductor portion [and the]. The

stress cushioning layer, lead wire portion, conductor protective layer, and external electrodes have a means for forming each end face on the end surface of the semiconductor elements inside the cutting scribe line and exposing the range from the end face on the end surface of the semiconductor elements to the inside of the scribe line.

[0011]

To accomplish the above object, the semiconductor device of the present invention has semiconductor elements obtained by cutting a semiconductor wafer, having an integrated circuit and an electrode pad formed on one side thereof, along the cutting scribe line; a semiconductor element protective layer installed on the semiconductor elements; a stress cushioning layer installed on the semiconductor element protective layer; a first opening formed in the semiconductor element protective layer on the electrode pad; a second opening formed in the stress cushioning layer on the electrode pad; a lead wire portion extending to the top of the stress cushioning layer through the first opening and second opening, respectively, from the electrode pad; external electrodes arranged on the lead wire portion on the top of the stress cushioning layer; and a conductor protective layer installed on the stress cushioning layer, excluding the external electrode arranged portion, and on the conductor portion [and the]. The semiconductor element protective layer, stress cushioning layer, lead wire portion, conductor protective layer, and external electrodes have a



means for forming each end face on the end surface of the semiconductor elements inside the cutting scribe line and exposing the range from the end face on the end surface of the semiconductor elements to the inside of the scribe line.

5 [0012]

To accomplish the above object, the semiconductor device manufacturing method of the present invention has [a means for manufacturing a semiconductor device through] a first step of forming a plurality of semiconductor elements having an  
10 integrated circuit and an electrode pad on the circuit forming surface of a semiconductor wafer[,]; a second step of forming a stress cushioning layer on a plurality of semiconductor elements[,]; a third step of forming an opening in the electrode pad of the stress cushioning layer and forming a  
15 notch wider than the width of the scribe line in the stress cushioning layer on the cutting scribe line of the semiconductor wafer[,]; a fourth step of forming a lead wire portion extending from the electrode pad to the stress cushioning layer via the opening[,]; a fifth step of forming a  
20 conductor protective layer which covers the stress cushioning layer and lead wire portion and has an external electrode connection window portion on the lead wire portion and a notch at the position corresponding to the notch of the stress cushioning layer[,]; a sixth step of forming an external  
25 electrode in the external electrode connection window portion[,]; and a seventh step of cutting the semiconductor wafer along the cutting scribe line [and], thereby obtaining a

plurality of semiconductor [devicees] devices in minimum units.

[0013]

To accomplish the above object, the semiconductor device  
5 manufacturing method of the present invention has [a means for  
manufacturing a semiconductor device through] a first step of  
forming a plurality of semiconductor elements having an  
integrated circuit and an electrode pad on the circuit forming  
surface of a semiconductor wafer[,]; a second step of forming  
10 a semiconductor element protective layer on a plurality of  
semiconductor elements[,]; a third step of forming a first  
opening in the electrode pad of the semiconductor element  
protective layer and forming a notch wider than the width of  
the scribe line in the semiconductor element protective layer  
15 on the cutting scribe line of the semiconductor wafer[,]; a  
fourth step of forming a stress cushioning layer on the  
semiconductor element protective layer[,]; a fifth step of  
forming a second opening in the electrode pad of the stress  
cushioning layer and forming a notch at the position  
20 corresponding to the notch of the semiconductor element  
protective layer in the stress cushioning layer on the cutting  
scribe line of the semiconductor wafer[,]; a sixth step of  
forming a lead wire portion extending from the electrode pad  
to the stress cushioning layer via the first and second  
25 openings[,]; a seventh step of forming a conductor protective  
layer, which covers the stress cushioning layer and lead wire  
portion and has an external electrode connection window

portion on the lead wire portion and a notch at the position corresponding to the notch of the stress cushioning layer[,]; an eighth step of forming an external electrode in the external electrode connection window portion[,]; and a ninth  
5 step of cutting the semiconductor wafer along the cutting scribe line [and], thereby obtaining a plurality of semiconductor [devicees] devices in minimum units.

[0014]

According to each [means] feature mentioned above, each  
10 end face of the stress cushioning layer and conductor protective layer, or each end face of the semiconductor element protective layer, stress cushioning layer, and conductor protective layer in the end face area of each semiconductor element, is formed so as to be positioned inside  
15 the semiconductor wafer cutting scribe line and exposed within the range from the end face of each semiconductor element to the inside of the scribe line, so that when a semiconductor wafer is to be cut along the semiconductor wafer cutting scribe line, the semiconductor wafer can be cut by surely  
20 recognizing the positioning marks [put] located on the semiconductor wafer [and], whereby defective semiconductor packages due to a displacement of the cutting position of each obtained semiconductor device can be eliminated.

[0015]

25 Further, according to each [means] feature mentioned above, when each semiconductor device is to be obtained by cutting a semiconductor wafer, the cut portion of each

semiconductor device is formed [in] to have a single-layer structure only of a semiconductor element; and, even if mechanical stress is generated at the time of cutting of the semiconductor wafer, the mechanical stress is just applied to the single-layer structure, so that a plurality of resin layers will not be peeled off by the mechanical stress.

[0016]

Furthermore, according to each [means] feature mentioned above, when each semiconductor device is to be mounted, even if thermal stress is generated due to great changes [of] in the environmental temperature and the thermal stress is applied to a plurality of resin layers, a large mechanical stress is not applied to the plurality of resin layers when the semiconductor wafer is cut [and], so that the plurality of resin layers are [little] hardly damaged, [so] with the result that none of the plurality of resin layers will be peeled off [not at all] or very little peeling will occur due to thermal stress.

[0017]

As mentioned above, according to each [means] feature mentioned above, the semiconductor [devicees are] devices will not be damaged at [not] all or very little damage will occur due to application of mechanical stress and thermal stress, [and] so that the reliability of the semiconductor [devicees] devices can be enhanced, and the production yield rate of the semiconductor [devicees] devices can be increased.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a first embodiment of the present invention.

5        Fig. 2 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a second embodiment of the present invention.

10       Fig. 3 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device of the third embodiment [of the] according to a present invention.

15       Fig. 4 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a fourth embodiment of the present invention.

20       Fig. 5 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a fifth embodiment of the present invention.

Fig. 6 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a sixth embodiment of the present invention.

25       Fig. 7 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a seventh embodiment of the

present invention.

Fig. 8 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a eighth embodiment of the present invention.

Fig. 9 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a ninth embodiment of the present invention.

Fig. 10 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a tenth embodiment of the present invention.

Fig. 11 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a eleventh embodiment of the present invention.

Fig. 12 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a twelfth embodiment of the present invention.

Fig. 13 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a thirteenth embodiment of the present invention.

Fig. 14 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor

device [of the] according to a fourteenth embodiment of the present invention.

Fig. 15 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a fifteenth embodiment of the present invention.

Fig. 16 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a sixteenth embodiment of the present invention.

Fig. 17 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a seventeenth embodiment of the present invention.

Fig. 18 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a eighteenth embodiment of the present invention.

Fig. 19 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a nineteenth embodiment of the present invention.

Fig. 20 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a twentieth embodiment of the present invention.

Fig. 21 is cross sectional view showing the constitution

of [the essential] a typical section of the semiconductor device [of the] according to a twenty-first embodiment of the present invention.

5 Fig. 22 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a twenty-second embodiment of the present invention.

10 Fig. 23 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a twenty-third embodiment of the present invention.

15 Fig. 24 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a twenty-fourth embodiment of the present invention.

Fig. 25 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a twenty-fifth embodiment of the present invention.

20 Fig. 26 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a twenty-sixth embodiment of the present invention.

25 Fig. 27 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a twenty-seventh embodiment of the present invention.



Fig. 28 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a twenty-eighth embodiment of the present invention.

5        Fig. 29 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a twenty-ninth embodiment of the present invention.

10       Fig. 30 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a thirtieth embodiment of the present invention.

15       Fig. 31 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a thirty-first embodiment of the present invention.

20       Fig. 32 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a thirty-second embodiment of the present invention.

Fig. 33 is cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a thirty-third embodiment of the present invention.

25       Fig. 34 is cross sectional view showing the constitution of a typical section of a semiconductor device [as] representing a first comparison example.

Fig. 35 is cross sectional view showing the constitution of a typical section of a semiconductor device [as] representing a second comparison example.

5 Fig. 36 is cross sectional view showing the constitution of a typical section of a semiconductor device [as] representing a third comparison example.

Fig. 37 is cross sectional view showing the constitution of a typical section of a semiconductor device [as] representing a fourth comparison example.

10 Fig. 38 is a view showing a semiconductor device according to first, third, forth, sixth, seventh and ninth embodiments of this invention and illustrates the structure of its substantial part.

15 Fig. 39 is a view showing a semiconductor device according to second, fifth and eighth embodiments of this invention and illustrates the structure of its substantial part.

20 Fig. 40 is a view showing a semiconductor device according to tenth, fourteenth, sixteenth, seventeenth, eighteenth, twenty-second, twenty-sixth, twenty-eighth, twenty-ninth, thirtieth, thirty-second and thirty-third embodiments of this invention and illustrates the structure of its substantial part.

25 Fig. 41 is a view showing a semiconductor device according to eleventh, thirteenth, nineteenth, twenty-first, twenty-third and twenty-fifth embodiments of this invention and illustrates the structure of its substantial part.

Fig. 42 is a view showing a semiconductor device according to twelfth, twentieth, twenty-fourth and thirty-first embodiments of this invention and illustrates the structure of its substantial part.

5 Fig. 43 is a view showing a semiconductor device according to fifteenth and twenty-seventh embodiments of this invention and illustrates the structure of its substantial part.

10 Fig. 44 is a view showing a semiconductor device which constitutes first, second, third and fourth comparison examples and illustrates the structure of its substantial part.

[0018]

#### DETAILED DESCRIPTION OF THE INVENTION

15 The embodiments of the semiconductor device and manufacturing method thereof of the present invention will be explained hereunder with reference to the accompanying drawings.

[0019]

20 Fig. 1 is a cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a first embodiment of the present invention. Also, Fig. 38 is a view showing a semiconductor device according to a first embodiment of this invention and illustrates the structure of its substantial part. Further,  
25 Fig. 1 shows a sectional view taken along lines A-B in Fig. 38.

[0020]

In Fig. 1 and Fig. 38, numeral 1 indicates a semiconductor element, 1(1) denotes an exposed end face of the semiconductor element 1, 2 denotes an electrode pad, 3 denotes a stress cushioning layer, 3(1) denotes an opening formed in the stress cushioning layer 3, 4 denotes a lead wire portion, 5 a conductor protective layer, 5(1) denotes a plurality of windows installed in the conductor protective layer 5, and 6 denotes an external electrode.

[0021]

The semiconductor element 1 has the electrode pad 2 and an integrated circuit portion, which is not shown in the drawing, which are arranged on one side thereof, and, the semiconductor element 1 has an exposed end face 1(1). The stress cushioning layer 3 is formed on one side of the semiconductor element 1 and has [the] an opening 3(1) [on] above the [electron] electrode pad 2 and a slit (no drawing No. is assigned) [reaching] extending to the bottom on the end face 1(1). The lead wire portion 4 is formed within the range from the electrode pad 2 [to] along a part of the stress cushioning layer 3 [via] within the opening 3(1). The conductor protective layer 5 is formed on the stress cushioning layer 3, including the lead wire portion 4, and has a plurality of windows 5(1) on a part of the lead wire portion 4, and a slit (no drawing No. is assigned) [reaching] extends to the bottom of the conductor protective layer 5 at the position corresponding to the slit of the stress cushioning layer 3 on the end face 1(1). The external electrodes 6 are

arranged on the lead wire portion 4 via each of the window portions 5(1).

[0022]

5 In this case, the end face of the stress cushioning layer 3 [obtained by forming of] formed by the slit and the end face of the conductor protective layer 5 obtained by forming [of] the slit are positioned on the same surface, and the exposed end face 1(1) is formed within the range from the end face of the semiconductor element 1 to the end face of the stress  
10 cushioning layer 3 and the end face of the conductor protective layer 5 positioned on the same surface. The end face of the stress cushioning layer 3 and the end face of the conductor protective layer 5 are positioned slightly inside the cutting scribe line formed on a semiconductor wafer (not  
15 shown in the drawing) which will be described later.

[0023]

Next, the semiconductor device manufacturing method [of] according to the first embodiment will be described. A plurality of semiconductor [devicees] devices are manufactured  
20 at the same time by cutting a semiconductor wafer; and, on the semiconductor wafer, positioning marks (not shown in the drawing) are formed at the intersections of the scribe lines, which [are] constitute a cutting portion [and semiconductor devicees]. Semiconductor devices are formed, respectively, on  
25 one side of the semiconductor wafer enclosed by the positioning marks, and then the semiconductor wafer is cut along the positioning marks, [thereby] whereby a plurality of

semiconductor [devicees] devices are manufactured.

[0024]

Firstly, positioning marks made of aluminum (Al) indicating an intersection of scribe lines are formed on one side of a semiconductor wafer made of silicon (Si); and, in the areas enclosed by the positioning marks, the electrode pads 2 of aluminum (Al) are formed [respectively]. Then, and an integrated circuit portion (not shown in the drawing) is formed thereon.

[0025]

Next, on the one side of the semiconductor wafer [with] on which the positioning marks and electrode pads 2 are formed, the stress cushioning layer 3, including the opening 3(1) having a gently-inclined rising portion, is formed using [the] a mask printing method. In this case, the printing mask to be used by the mask printing method has the same structure as that of the printing mask used for solder paste printing in a printed circuit board, and a so-called contact print for positioning and closely adhering a semiconductor wafer pattern and a printing mask and executing squeeze printing in this state is used. During printing, the whole squeeze surface of the printing mask is coated with paste at the first squeezing, and the opening of the printing mask is filled at the second squeezing, [and] after which excessive paste is removed, and then the printing mask is removed from the semiconductor wafer, and the mask print is completed. Thereafter, the semiconductor wafer with paste print-coated thereon is heated

stepwise using a hot plate or a heating oven, and the print-coated paste is hardened, [and] whereby the stress cushioning layer 3 having the opening 3(1) is formed.

[0026]

5           The material to be used to form the stress cushioning layer 3 is a pasty polyimide material and is hardened by heating after print-coating. The pasty polyimide material has satisfactory print-coating characteristics, such as a viscosity of 530 Pa-s and a thixotropy factor of 2.8. When  
10   such a pasty polyimide material is used, the wetting spread is made smaller [and], so that the stress cushioning layer 3 having the opening 3(1) as shown in Fig. 1 can be formed. When a stress cushioning layer 3 having a necessary thickness cannot be obtained by one mask printing, by repeating print-  
15   coating and hardening of the coated material several times, a predetermined thickness can be obtained.

[0027]

          In this case, when a pasty polyimide material is used [as a forming material of] to form the stress cushioning layer 3  
20   and a metal mask with a thickness of 65  $\mu\text{m}$  is used as a printing mask, by print-coating and hardening [of] the coated material two times, a stress cushioning layer 3 with a thickness of 50  $\mu\text{m}$  can be obtained. The hardening conditions in this case are sure that the material is print-coated  
25   [firstly] at first, heated on a hot plate at 100°C for 10 minutes, heated and hardened at 150°C for 10 minutes, then print-coated [secondarily] again, heated on the hot plate at

200°C for 25 minutes, and then heated and hardened in a  
thermostatic chamber at 250°C for 60 minutes.

[0028]

In the first embodiment, the stress cushioning layer 3 is  
5 formed using a pasty polyimide material. However, any low  
elastic resin material which can ensure the viscoelastic  
characteristics necessary for mask printing and withstand this  
manufacturing process from the viewpoint of the  
characteristics[, it] may be used.

10 [0029]

Next, a scribe line with a width of 200  $\mu\text{m}$  formed on a  
semiconductor wafer by laser processing using a carbon dioxide  
laser is exposed. In this case, a slit with a width of 400  $\mu\text{m}$   
reaching the bottom of the stress cushioning layer 3 is formed  
15 in the stress cushioning layer 3 [formed on] at the end  
surface 1(1) and the positioning marks of the semiconductor  
wafer formed on the end surface 1(1) are exposed via this  
slit.

[0030]

20 Then, a chromium (Cr) film with a thickness of 500 Å is  
deposited on the stress cushioning layer 3, including the  
electrode pad 2 and a copper (Cu) film with a thickness of 0.5  
 $\mu\text{m}$  is deposited on it. A negative type photosensitive resist  
is spin-coated on the obtained deposited film, prebaked,  
25 exposed, and developed, and a resist wiring pattern with a  
thickness of 15  $\mu\text{m}$  is formed. A copper (Cu) film with a  
thickness of 10  $\mu\text{m}$  is formed by electroplating inside the



formed wiring pattern<sub>1</sub> and a nickel (Ni) film with a thickness of 2  $\mu\text{m}$  is formed on it by electroplating. Thereafter, the resist is peeled off using a release liquid, and the copper (Cu) film among the deposited films is etched by an ammonium persulfate/sulfuric acid series solution[,]<sub>1</sub> and<sub>1</sub> furthermore, the chromium (Cr) film among the deposited films is etched by a potassium permanganate series solution, and the lead wire portion 4 is formed.

[0031]

When the lead wire portion 4 formed at this point of time [is] was evaluated [on] as to its suitability, no unsuitable (defective) lead wire portions [are] were found at all among all the evaluated ones.

[0032]

Next, the stress cushioning layer 3 including the lead wire portion 4 is coated with photosensitive solder resist varnish by screen printing, and the coated film is dried at 80°C for 20 minutes, exposed and developed using a predetermined pattern, and heated and hardened at 150°C for one hour, and the conductor protective layer 5 is formed. The formed conductor protective layer 5 has a plurality of window portions 5(1) on a part of the lead wire portion 4 and a slit (no drawing number is assigned) reaching the bottom of the conductor protective layer 5 at the position coinciding with the slit forming position of the stress cushioning layer 3 on the scribe line.

[0033]

Next, a gold (Au) plating film [with] having a thickness of 0.1  $\mu\text{m}$  is formed by replacement plating on the nickel (Ni) film of the lead wire portion 4, which is exposed via the windows 5(1). Thereafter, flux is coated on the gold (Au) plating film using a metal mask, and solder balls of Sn-Ag-Cu series with a diameter of about 0.35 mm are put on it[,]; and, the solder balls are heated in an infrared reflow furnace at 260°C for 10 seconds, [and] whereby the external electrodes 6 are formed.

[0034]

Finally, by checking the positioning marks formed on the end surface 1(1) of the semiconductor element 1, that is, on the semiconductor wafer by transmission, the semiconductor wafer is cut by a dicing saw [with] having a thickness of 0.2 mm along the scribe line [and], whereby a plurality of semiconductor [devicees] devices are manufactured.

[0035]

The semiconductor [devicees] devices of the first embodiment manufactured by this method [are] were subjected to [the] an appearance inspection immediately after dicing, and it [is] was found that the end area of the semiconductor element 1, including the plural-layer forming portion [is], was not damaged at all during dicing [and], so that there [are] were no defective semiconductor packages produced at all.

[0036]

Samples of a predetermined number [are] were extracted

from the semiconductor [devicees] devices of the first embodiment manufactured in this way, and a temperature test [is] was executed for each of the extracted samples [that] in which a temperature cycle of conditioning at -55°C for 10 minutes and conditioning at 125°C for 10 minutes is repeated 1000 times[, and each]. Each sample [is] was subjected to [the] appearance inspection after the temperature test [is] was executed, and it [is] was found that the plural-layer forming portion of the end area of the semiconductor element 1 [is] was not damaged during dicing[, thus]. Thus, the interface of the plural-layer forming portion [is] was not peeled off and no defective samples [are] were generated at all.

[0037]

Fig. 2 is a cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a second embodiment of the present invention. Also, Fig. 39 is a view showing a semiconductor device according to a second embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 2 shows a sectional view taken along lines A-B in Fig. 39.

[0038]

In Fig. 2 and Fig. 39, numeral 3(2) indicates an exposed end surface of the stress cushioning layer 3 and with respect to the other numerals, the same [numeral is] numerals are assigned to each of the same components as those shown in Fig.

1.

[0039]

The constituent difference between the aforementioned semiconductor device of the first embodiment (hereinafter[,]  
5 referred to as the first embodiment device) and the semiconductor device of the second embodiment (hereinafter[,]  
referred to as the second embodiment device) is only [a point]  
that, with respect to the constitution of the slit portion of  
the stress cushioning layer 3 on the end surface 1(1) of the  
10 semiconductor element 1 and the slit portion of the conductor  
protective layer 5, the first embodiment device is structured  
so that the end face of the stress cushioning layer 3 and the  
end face of the conductor protective layer 5 are [installed]  
located on the same plane, while the second embodiment device  
15 is structured so that the end face of the conductor protective  
layer 5 is [positioned on the inside] displaced inwardly  
compared with the end face of the stress cushioning layer 3,  
and [the] an exposed end surface 3(2) is [installed] located  
on the stress cushioning layer 3 [and there]. There are no  
20 other constituent differences between the first embodiment  
device and the second embodiment device. Therefore, an  
additional explanation [on] of the constitution of the second  
embodiment device will be omitted.

[0040]

25 The [manufacturing] method of manufacture of the second  
embodiment device is the same as [the manufacturing method]  
that of the first embodiment device, so that [the] an

explanation [on] of the [manufacturing] method of manufacture  
of the second embodiment device will be also omitted.

[0041]

5 The second embodiment device manufactured by such a  
method [is evaluated on the suitability immediately after  
forming of the lead wire portion 4 and there are no unsuitable  
(defective) lead wire portions found at all in all the  
evaluated ones. When the appearance inspection is executed  
immediately after dicing, it is found that there are no  
10 defective semiconductor packages at all and when the same  
temperature test as that performed for the first embodiment  
device [is executed] was carried out, it [is] was also found  
that there [are] were no defective samples at all.

[0042]

15 Fig. 3 is a cross sectional view showing the constitution  
of [the essential] a typical section of the semiconductor  
device [of the] according to a third embodiment of the present  
invention. Also, Fig. 38 is a view showing a semiconductor  
device according to a third embodiment of this invention and  
20 illustrates the structure of its substantial part. Further,  
Fig. 3 shows a sectional view taken along lines A-B in Fig.  
38.

[0043]

In Fig. 3 and Fig. 38, the same [numeral is] numerals are  
25 assigned to each of the same components as those shown in Fig.  
1.

[0044]

The constituent difference between the aforementioned semiconductor device of the first embodiment (hereinafter[, referred to as the first embodiment device again) and the semiconductor device of the third embodiment (hereinafter[, referred to as the third embodiment device) is only [a point] that, with respect to the constitution of the slit portion of the stress cushioning layer 3 and the slit portion of the conductor protective layer 5 on the end surface 1(1) of the semiconductor element 1, the first embodiment device is structured so that the end face of the stress cushioning layer 3 and the end face of the conductor protective layer 5 are installed on the same plane, while the third embodiment device is structured so that the end face of the conductor protective layer 5 is positioned [on the] outside [compared with] of and covers the end face of the stress cushioning layer 3 [and] so that the outside part of the conductor protective layer 5 [of the outside part] reaches the end surface 1(1) [and there]. There are no other constituent differences between the first embodiment device and the third embodiment device. Therefore, additional explanation [on] of the constitution of the third embodiment device will be omitted.

[0045]

The [manufacturing] method of manufacture of the third embodiment device is the same as [the manufacturing method] that of the first embodiment device, so that [the] an explanation [on] of the [manufacturing] method of manufacture of the third embodiment device will be [also] omitted.

[0046]

The third embodiment device manufactured by such a method [is] was evaluated [on the] as to its suitability immediately after forming [of] the lead wire portion 4, and [there are] no unsuitable (defective) lead wire portions were found at all in all the evaluated [ones] devices. When [the] an appearance inspection [is executed] was performed immediately after dicing, it [is] was found that there [are] were no defective semiconductor packages at all, and when the same temperature test as that performed for the first embodiment device [is executed] was carried out, it [is also] was found that there [are] were no defective samples at all.

[0047]

Fig. 4 is a cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device according to a fourth embodiment of the present invention. Also, Fig. 38 is a view showing a semiconductor device according to a forth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 4 shows a sectional view taken along lines A-B in Fig. 38.

[0048]

In Fig. 4 and Fig. 38, the same [numeral is] numerals are assigned to each of the same components as those shown in Fig. 1.

[0049]

The constituent difference between the aforementioned

semiconductor device of the first embodiment (hereinafter[,]  
referred to as the first embodiment device again) and the  
semiconductor device of the fourth embodiment (hereinafter[,]  
referred to as the fourth embodiment device) is only [a point]  
5 that, with respect to the constitution of the end area of the  
stress cushioning layer 3 and the end area of the conductor  
protective layer 5, the first embodiment device is structured  
so that a slit portion is formed in the stress cushioning  
layer 3, and a slit portion is also formed in the conductor  
10 protective layer 5, and their end faces are [installed]  
disposed on the same plane, while the fourth embodiment device  
is structured so that a tapered portion becoming thinner  
[taperingly] toward the end face is formed on the stress  
cushioning layer 3, and a slit portion is formed in the  
15 conductor protective layer 5, [and] such that the end (end  
face) of the tapered portion and the end face of the slit  
portion are installed on the same plane, and the thickness of  
the conductor protective layer 5 [replenishes to] compensates  
for changes in the thickness of the tapered portion [and  
20 there]. There are no other constituent differences between  
the first embodiment device and the fourth embodiment device.  
Therefore, additional explanation [on] of the constitution of  
the fourth embodiment device will be omitted.

[0050]

25 As compared with the [manufacturing] method of  
manufacture of the first embodiment device, the manufacturing  
method of the fourth embodiment device has only a difference



in that, with respect to the forming means of the stress cushioning layer 3, the manufacturing method of the first embodiment device forms the stress cushioning layer 3 including the opening 3(1) having a gently-inclined rising portion using the mask printing method and then forms a slit portion in the stress cushioning layer 3 by laser processing, while the manufacturing method of the fourth embodiment device forms the stress cushioning layer 3 including the opening 3(1) having a gently-inclined rising portion and a tapered portion becoming thinner [taperingly] toward the end face using the mask printing method and does not perform the subsequent laser processing for the stress cushioning layer 3 [and there]. There are no other differences between the manufacturing method of the first embodiment device and the manufacturing method of the fourth embodiment device. Therefore, additional explanation [on] of the manufacturing method of the fourth embodiment device will be omitted.

[0051]

The fourth embodiment device manufactured by such a method [is] was evaluated [on the] as to its suitability immediately after forming [of] the lead wire portion 4, and [there are] no unsuitable (defective) lead wire portions were found at all in all the evaluated [ones] devices. When [the] an appearance inspection [is executed] was performed immediately after dicing, it [is] was found that there [are] were no defective semiconductor packages at all, and when the same temperature test as that performed for the first

embodiment device [is executed] was carried out, it [is also]  
was found that there [are] were no defective samples at all.  
[0052]

Fig. 5 is a cross sectional view showing the constitution  
5 of [the essential] a typical section of the semiconductor  
device [of the] according to a fifth embodiment of the present  
invention. Also, Fig. 39 is a view showing a semiconductor  
device according to a fifth embodiment of this invention and  
illustrates the structure of its substantial part. Further,  
10 Fig. 5 shows a sectional view taken along lines A-B in Fig.  
39.

[0053]

In Fig. 5 and Fig. 39, the same [numeral is] numerals are  
assigned to each of the same components as those shown in  
15 Figs. 2 and 4.

[0054]

The constituent difference between the aforementioned  
semiconductor device of the fourth embodiment (hereinafter[,]  
referred to as the fourth embodiment device again) and the  
20 semiconductor device of the fifth embodiment (hereinafter[,]  
referred to as the fifth embodiment device) is only [a point]  
that with respect to the constitution of the end (end face) of  
the stress cushioning layer 3 and the end face of the  
conductor protective layer 5, the fourth embodiment device is  
25 structured so that the end (end face) of the stress cushioning  
layer 3 and the end face of the conductor protective layer 5  
are [installed] disposed on the same plane, while the fifth

embodiment device is structured so that the end face of the conductor protective layer 5 is [positioned on the inside compared with] shifted inwardly of the end (end face) of the stress cushioning layer 3, and [the] an exposed end surface 3(2) is [installed] provided on the stress cushioning layer 3 [and there]. There are no other constituent differences between the fourth embodiment device and the fifth embodiment device. Therefore, additional explanation [on] of the constitution of the fifth embodiment device will be omitted.

[0055]

The [manufacturing] method of manufacture of the fifth embodiment device is the same as [the manufacturing method] that of the fourth embodiment device, except [a point] that the mask printing method is used for forming the conductor protective layer 5 [in stead] instead of the screen printing method[, so that the]. Thus, an explanation of the manufacturing method of the fifth embodiment device will be [also] omitted.

[0056]

The fifth embodiment device manufactured by such a method [is] was evaluated [on the] as to its suitability immediately after forming [of] the lead wire portion 4, and [there are] no unsuitable (defective) lead wire portions were found at all in all the evaluated [ones] devices. When [the] an appearance inspection [is executed] was performed immediately after dicing, it [is] was found that there [are] were no defective semiconductor packages at all, and when the same temperature

test as that performed for the first embodiment device [is executed] was carried out, it [is also] was found that there [are] were no defective samples at all.

[0057]

5            Fig. 6 is a cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a sixth embodiment of the present invention. Also, Fig. 38 is a view showing a semiconductor device according to a sixth embodiment of this invention and  
10 illustrates the structure of its substantial part. Further, Fig. 6 shows a sectional view taken along lines A-B in Fig. 38.

[0058]

          In Fig. 6 and Fig. 38, the same [numeral is] numerals are  
15 assigned to each of the same components as those shown in Fig. 4.

[0059]

          The constituent difference between the aforementioned semiconductor device of the fourth embodiment (hereinafter[,]  
20 referred to as the fourth embodiment device again) and the semiconductor device of the sixth embodiment (hereinafter[,]  
referred to as the sixth embodiment device) is only [a point] that, with respect to the constitution of the end (end face) of the stress cushioning layer 3 and the end face of the  
25 conductor protective layer 5, the fourth embodiment device is structured so that the end (end face) of the stress cushioning layer 3 and the end face of the conductor protective layer 5

are [installed] disposed on the same plane, while the sixth embodiment device is structured so that the end face of the conductor protective layer 5 is positioned [on the] outside [compared with] of and covers the end (end face) of the stress cushioning layer 3 [and] so that the conductor protective layer 5 of the outside part reaches the end surface 1(1) [and there]. There are no other constituent differences between the fourth embodiment device and the sixth embodiment device. Therefore, additional explanation [on] of the constitution of the sixth embodiment device will be omitted.

[0060]

The [manufacturing] method of manufacture of the sixth embodiment device is the same as [the manufacturing method] that of the fourth embodiment device, so that [the] an explanation [on] of the [manufacturing] method of manufacture of the sixth embodiment device will be [also] omitted.

[0061]

The sixth embodiment device manufactured by such a method [is] was evaluated [on the] as to its suitability immediately after forming [of] the lead wire portion 4, and [there are] no unsuitable (defective) lead wire portions were found at all in all the evaluated [ones] devices. When [the] an appearance inspection [is executed] was performed immediately after dicing, it [is] was found that there [are] were no defective semiconductor packages at all, and when the same temperature test as that performed for the first embodiment device [is executed] was carried out, it [is also] was found that there

[are] were no defective samples at all.

[0062]

Fig. 7 is a cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a seventh embodiment of the present invention. Also, Fig. 38 is a view showing a semiconductor device according to a seventh embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 7 shows a sectional view taken along lines A-B in Fig. 38.

[0063]

In Fig. 7 and Fig. 38, the same [numeral is] numerals are assigned to each of the same components as those shown in Fig. 4.

[0064]

The constituent difference between the aforementioned semiconductor device of the fourth embodiment (hereinafter[, ] referred to as the fourth embodiment device again) and the semiconductor device of the seventh embodiment (hereinafter[, ] referred to as the seventh embodiment device) is only [a point] that, with respect to the constitution of the end area of the conductor protective layer 5, the fourth embodiment device is structured so that a slit portion is formed in the conductor protective layer 5, and the end face of the conductor protective layer 5 is almost perpendicular to the end surface 1(1), while the seventh embodiment device is structured so that an inclined surface becoming thinner

linearly toward the end face of the conductor protective layer 5 is formed [and there]. There are no other constituent differences between the fourth embodiment device and the seventh embodiment device. Therefore, additional explanation [on] of the constitution of the seventh embodiment device will be omitted.

[0065]

When the [manufacturing] method of manufacture of the seventh embodiment device is compared with [the manufacturing method] that of the fourth embodiment device, the difference is only [a point] that, with respect to the forming means of the conductor protective [p]layer 5, the manufacturing method of the fourth embodiment device forms the conductor protective layer 5 including the opening 3(1) having a gently-inclined rising portion and a slit portion having an end face almost perpendicular to the end surface 1(1) using the screen printing method, while the manufacturing method of the seventh embodiment device forms the conductor protective layer 5 including the opening 3(1) having a gently-inclined rising portion and an inclined surface having a linearly-inclined rising portion using the mask printing method [and there]. There are no other differences between the manufacturing method of the fourth embodiment device and the manufacturing method of the seventh embodiment device. Therefore, additional explanation [on] of the manufacturing method of the seventh embodiment device will be omitted.

[0066]

The seventh embodiment device manufactured by such a method [is] was evaluated [on the] as to its suitability immediately after forming [of] the lead wire portion 4, and [there are] no unsuitable (defective) lead wire portions were found at all in all the evaluated [ones] devices. When the appearance inspection [is executed] was performed immediately after dicing, it [is] was found that there [are] were no defective semiconductor packages at all, and when the same temperature test as that performed for the first embodiment device [is executed] was carried out, it [is] was also found that there [are no] were defective samples at all.

[0067]

Fig. 8 is a cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to an eighth embodiment of the present invention. Also, Fig. 39 is a view showing a semiconductor device according to an eighth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 8 shows a sectional view taken along lines A-B in Fig. 39.

[0068]

In Fig. 8 and Fig. 39, the same [numeral is] numerals are assigned to each of the same components as those shown in Figs. 5 and 7.

[0069]

The constituent difference between the aforementioned semiconductor device of the seventh embodiment (hereinafter[,]



referred to as the seventh embodiment device again) and the semiconductor device of the eighth embodiment (hereinafter[, referred to as the eighth embodiment device) is only [a point] that, with respect to the constitution of the end (end face) of the stress cushioning layer 3 and the end (end face) of the conductor protective layer 5, the seventh embodiment device is structured so that the end (end face) of the stress cushioning layer 3 and the end (end face) of the conductor protective layer 5 are [installed] disposed on the same plane, while the eighth embodiment device is structured so that the end face of the conductor protective layer 5 is positioned [on the inside compared with] inwardly of the end (end face) of the stress cushioning layer 3 [and the] so that an exposed end surface 3(2) is [installed] provided on the stress cushioning layer 3 [and there]. There are no other constituent differences between the seventh embodiment device and the eighth embodiment device. Therefore, additional explanation [on] of the constitution of the eighth embodiment device will be omitted.

[0070]

The [manufacturing] method of manufacture of the eighth embodiment device is the same as [the manufacturing method] that of the seventh embodiment device, except [a point] that the screen printing method is used for forming the conductor protective layer 5 [in stead] instead of the mask printing method[, so that the]. Thus, an explanation of the manufacturing method of the eighth embodiment device will be

[also] omitted.

[0071]

The eighth embodiment device manufactured by such a method [is] was evaluated [on the] as to its suitability immediately after forming [of] the lead wire portion 4, and [there are] no unsuitable (defective) lead wire portions were found at all in all the evaluated [ones] devices. When [the] an appearance inspection [is] was executed immediately after dicing, it is found that there [are] were no defective semiconductor packages at all, and when the same temperature test as that performed for the first embodiment device [is executed] was carried out, it [is also] was found that there [are] were no defective samples at all.

[0072]

Fig. 9 is a cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a ninth embodiment of the present invention. Also, Fig. 38 is a view showing a semiconductor device according to a ninth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 9 shows a sectional view taken along lines A-B in Fig. 38.

[0073]

In Fig. 9 and Fig. 38, the same [numeral is] numerals are assigned to each of the same components as those shown in Fig. 7.

[0074]

The constituent difference between the aforementioned semiconductor device of the seventh embodiment (hereinafter[, referred to as the seventh embodiment device again) and the semiconductor device of the ninth embodiment (hereinafter[, referred to as the ninth embodiment device) is only [a point] that, with respect to the constitution of the end (end face) of the stress cushioning layer 3 and the end (end face) of the conductor protective layer 5, the seventh embodiment device is structured so that the end (end face) of the stress cushioning layer 3 and the end (end face) of the conductor protective layer 5 are [installed] disposed on the same plane, while the ninth embodiment device is structured so that the end face of the conductor protective layer 5 is positioned [on the] outside [compared with] of and covers the end (end face) of the stress cushioning layer 3 [and] so that the outside part of the conductor protective layer 5 [of the outside part] reaches the end surface 1(1) [and there]. There are no other constituent differences between the seventh embodiment device and the ninth embodiment device. Therefore, additional explanation [on] of the constitution of the ninth embodiment device will be omitted.

[0075]

The [manufacturing] method of manufacture of the ninth embodiment device is the same as [the manufacturing method] that of the seventh embodiment device, so that [the] an explanation [on] of the manufacturing method of the ninth embodiment device will be [also] omitted.

[0076]

The ninth embodiment device manufactured by such a method [is] was evaluated [on the] as to its suitability immediately after forming [of] the lead wire portion 4, and [there are] no  
5 unsuitable (defective) lead wire portions were found at all in all the evaluated [ones] devices. When the appearance inspection [is executed] was performed immediately after dicing, it [is] was found that there [are] were no defective semiconductor packages at all, and when the same temperature  
10 test as that performed for the first embodiment device [is executed] carried out, it [is also] was found that there [are] were no defective samples at all.

[0077]

Fig. 10 is a cross sectional view showing the  
15 constitution of [the essential] a typical section of the semiconductor device [of the] according to a tenth embodiment of the present invention. Also, Fig. 40 is a view showing a semiconductor device according to a tenth embodiment of this invention and illustrates the structure of its substantial  
20 part. Further, Fig. 10 shows a sectional view taken along lines A-B in Fig. 40.

[0078]

In the following explanation, the semiconductor device of the tenth embodiment is referred to as the tenth embodiment  
25 device.

[0079]

In Fig. 10 and Fig. 40, numeral 7 indicates a

semiconductor element protective layer, and numeral 7(1) indicates an opening (first opening) formed in the semiconductor element protective layer 7[, and]. For the other elements, the same [numeral is] numerals are assigned to each of the same components as those shown in Fig. 1. In the following explanation, the opening 3(1) formed in the stress cushioning layer 3 in correspondence with the first opening 7(1) is assumed [as] to be a second opening.

[0080]

The semiconductor element protective layer 7 is formed on one side of the semiconductor element 1, where the electrode pad 2 and an integrated circuit portion, which are not shown in the drawing, are formed and arranged, and the first opening 7(1) is [installed on] located above the electrode pad 2[, and]. A a slit portion reaching the bottom of the semiconductor element protective layer 7 [is installed on] extends to the end surface 1(1) of the semiconductor element 1. The stress cushioning layer 3 is formed on the semiconductor element protective layer 7, and the second opening 3(1) is [installed in the] located at a position corresponding to the first opening 7(1) on the electrode pad 2[, and a]. A slit portion reaching the bottom of the stress cushioning layer 3 is installed on the end surface 1(1). The lead wire portion 4 is formed within the range from the electrode pad 2 to a part of the stress cushioning layer 3 via the first opening 7(1) and the second opening 3(1). The conductor protective layer 5 is formed on the stress

cushioning layer 3, including the lead wire portion, and a plurality of [window] windows 5(1) are formed in a part of the lead wire portion 4, [and] with a slit portion reaching the bottom of the conductor protective layer 5 [is] being formed on the end surface 1(1). The external electrodes 6 are formed and arranged on the lead wire portion 4 via the windows 5(1).  
[0081]

In this case, the end face of the semiconductor element protective layer 7 obtained by forming [of] the slit portion, the end face of the stress cushioning layer 3 obtained by forming [of] the slit portion, and the end face of the conductor protective layer 5 obtained by forming [of] the slit portion are positioned on the same plane, [respectively] and the exposed end surface 1(1) is formed within the range from the end face of the semiconductor element 1 to the end face of the semiconductor element protective layer 7, the end face of the stress cushioning layer 3, and the end face of the conductor protective layer 5, which are positioned on the same plane. The end face of the semiconductor element protective layer 7, the end face of the stress cushioning layer 3, and the end face of the conductor protective layer 5, which are [positioned] disposed on the same plane, are positioned slightly inside a cutting scribe line formed on [a] the semiconductor wafer.

[0082]

The [manufacturing] method of manufacture of the semiconductor device of the tenth embodiment will be described

hereunder.

[0083]

[Firstly] First, positioning marks made of aluminum (Al) indicating the intersection of scribe lines are formed on one side of a semiconductor wafer made of silicon (Si) or [others] materials, and the electrode pads 2 of aluminum (Al) are formed respectively in the areas enclosed by the positioning marks[, and]. Then, an integrated circuit portion (not shown in the drawing) is formed and arranged thereon.

[0084]

Next, on the one side of the semiconductor wafer on which the positioning marks and the electrode pads 2 are formed, negative photosensitive polyimide resin is coated by spin coating and the semiconductor wafer is dried on a hot plate at 75°C for 105 seconds and then at 90°C for 105 seconds[, then]. Then it is exposed using a predetermined mask, and heated again on the hot plate at 125°C for 60 seconds, and then developed. Thereafter, the semiconductor wafer is heated and cured in a nitrogen (N<sub>2</sub>) atmosphere at 350°C for 60 seconds [and the]. The semiconductor element protective layer 7 having the opening 7(1) on the electrode pad 2 and the slit portion [that] by which the end surface 1(1) of the semiconductor wafer 1 is exposed linearly as far as about 100 μm inside the end face of the semiconductor element 1 is formed.

[0085]

Next, the aluminum (Al) oxide film is removed from the

surface of the electrode pad 2 by sputter etching using argon (Ar) gas.

[0086]

5 The [forming] process of forming the stress cushioning layer 3 to be installed on the semiconductor element protective layer 7 thereafter, the [forming] process of forming the lead wire portion 4 reaching a part of the stress cushioning layer 3 from the electrode pad 2 via the first opening 7(1) and the second opening 3(1), the [forming]  
10 process of forming the conductor protective layer 5 to be installed on the stress cushioning layer 3 including the lead wire portion 4, the [forming] process of forming the external electrodes 6 to be formed on the lead wire portion 4, and the [cutting] process of cutting a semiconductor wafer are the  
15 same as the corresponding respective [forming] processes [of] used in the [manufacturing] method of manufacture of the first embodiment [device], so that additional explanation [on] of the [manufacturing] method of manufacture of the tenth embodiment semiconductor device will be omitted.

20 [0087]

The tenth embodiment device manufactured by such a method [is] was evaluated [on the] as to its suitability immediately after forming the lead wire portion 4, and [there are] no unsuitable (defective) lead wire portions were found at all in  
25 all the evaluated [ones] devices. When [the] an appearance inspection [is executed] was performed immediately after dicing, it [is] was found that there [are] were no defective



semiconductor packages at all, and when the same temperature test as that performed for the first embodiment device [is executed] was carried out, it [is also] was found that there [are] were no defective samples at all.

5 [0088]

Fig. 11 is a cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to an eleventh embodiment of the present invention. Also, Fig. 41 is a view  
10 showing a semiconductor device according to an eleventh embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 11 shows a sectional view taken along lines A-B in Fig. 41.

[0089]

15 In Fig. 11 and Fig. 41, the same [numeral is] numerals are assigned to each of the same components as those shown in Figs. 1 and 2.

[0090]

The constituent difference between the aforementioned  
20 semiconductor device of the tenth embodiment (hereinafter[, ] referred to as the tenth embodiment device again) and the semiconductor device of the eleventh embodiment (hereinafter[, ] referred to as the eleventh embodiment device) is only [a point] that, with respect to the constitution of  
25 the slit portions of the semiconductor element protective layer 7 and the stress cushioning layer 3 and the slit portion of the conductor protective layer 5 on the end surface 1(1) of

the semiconductor element 1, the tenth embodiment device is structured so that the end face of the semiconductor element protective layer 7, the end face of the stress cushioning layer 3, and the end face of the conductor protective layer 5 are [installed] disposed on the same plane, while the eleventh embodiment device is structured so that the end face of the semiconductor element protective layer 7 and the end face of the stress cushioning layer 3 are positioned on the same plane, [and] while the end face of the conductor protective layer 5 is positioned [on the inside] inwardly compared with the same plane, [and the] so that an exposed end surface 3(2) is [installed] provided on the stress cushioning layer 3 [and there]. There are no other constituent differences between the tenth embodiment device and the eleventh embodiment device. Therefore, additional explanation [on] of the constitution of the eleventh embodiment device will be omitted.

[0091]

The [manufacturing] method of manufacture of the eleventh embodiment device is the same as [the manufacturing method] of the tenth embodiment device, so that [the] an explanation on the [manufacturing] method of manufacture of the tenth embodiment device will be omitted.

[0092]

The eleventh embodiment device manufactured by such a method [is] was evaluated [on the] as to its suitability immediately after forming [of] the lead wire portion 4, and

[there are] no unsuitable (defective) lead wire portions were found at all in all the evaluated ones. When [the] an appearance inspection [is executed] was performed immediately after dicing, it [is] was found that there [are] were no defective semiconductor packages at all, and when the same temperature test as that performed for the first embodiment device [is executed] was carried out, it [is also] was found that there [are] were no defective samples at all.

[0093]

Fig. 12 is a cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to an twelfth embodiment of the present invention. Also, Fig. 42 is a view showing a semiconductor device according to a twelfth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 12 shows a sectional view taken along lines A-B in Fig. 42.

[0094]

In Fig. 12 and Fig. 42, numeral 7(2) indicates [the] an exposed end surface of the semiconductor element protective layer 7[ and]. For the other elements, the same [numeral is] numerals are assigned to each of the same components as those shown in Fig. 11.

[0095]

The constituent difference between the aforementioned semiconductor device of the eleventh embodiment (hereinafter[,] referred to as the first embodiment device

again) and the semiconductor device of the twelfth embodiment (hereinafter[, ] referred to as the twelfth embodiment device) is only [a point] that, with respect to the constitution of the [slip] slit portion of the semiconductor element protective layer 7 and the slit portion of the stress cushioning layer 3 on the end surface 1(1) of the semiconductor element 1, the eleventh embodiment device is structured so that the end face of the semiconductor element protective layer 7 and the end face of the stress cushioning layer 3 are [installed] disposed on the same plane, while the twelfth embodiment device is structured so that the end face of the stress cushioning layer 3 is positioned [on the inside] inwardly compared with the end face of the semiconductor element protective layer 7 [and the], so that an exposed end surface 7(2) is [installed] provided on the semiconductor element protective layer 7 [and there]. There are no other constituent differences between the eleventh embodiment device and the twelfth embodiment device. Therefore, additional explanation [on] of the constitution of the twelfth embodiment device will be omitted.

[0096]

The [manufacturing] method of manufacture of the twelfth embodiment device is the same as [the manufacturing method] that of the eleventh embodiment device, so that [the] an explanation [on] of the [manufacturing] method of manufacture of the twelfth embodiment device will be omitted.

[0097]

The twelfth embodiment device manufactured by such a method [is] was evaluated [on the] as to its suitability immediately after forming [of] the lead wire portion 4, and [there are] no unsuitable (defective) lead wire portions were found at all in all the evaluated [ones] devices. When [the] an appearance inspection [is executed] was performed immediately after dicing, it [is] was found that there [are] were no defective semiconductor packages at all, and when the same temperature test as that performed for the first embodiment device [is executed] was carried out, it [is also] was found that there [are] were no defective samples at all.

[0098]

Fig. 13 is a cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a thirteenth embodiment of the present invention. Also, Fig. 41 is a view showing a semiconductor device according to a thirteenth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 13 shows a sectional view taken along lines A-B in Fig. 41.

[0099]

In Fig. 13 and Fig. 41, the same [numeral is] numerals are assigned to each of the same components as those shown in Fig. 11.

[0100]

The constituent difference between the aforementioned semiconductor device of the eleventh embodiment

(hereinafter[,] referred to as the eleventh embodiment device again) and the semiconductor device of the thirteenth embodiment (hereinafter[,] referred to as the thirteenth embodiment device) is only [a point] that, with respect to the constitution of the [slip] slit portion of the semiconductor element protective layer 7 and the slit portion of the stress cushioning layer 3 on the end surface 1(1) of the semiconductor element 1, the eleventh embodiment device is structured so that the end face of the semiconductor element protective layer 7 and the end face of the stress cushioning layer 3 are [installed] disposed on the same plane, while the thirteenth embodiment device is structured so that the end face of the stress cushioning layer 3 is positioned [on the] outside [compared with] of and covers the end face of the semiconductor element protective layer 7 [and], so that the stress cushioning layer 3 of the outside part reaches the end surface 1(1) [and there]. There are no other constituent differences between the eleventh embodiment device and the thirteenth embodiment device. Therefore, additional explanation [on] of the constitution of the thirteenth embodiment device will be omitted.

[0101]

The [manufacturing] method of manufacture of the thirteenth embodiment device is the same as [the manufacturing method] that of the eleventh embodiment device, so that [the] an explanation [on] of the [manufacturing] method of manufacture of the thirteenth embodiment device will be

omitted.

[0102]

The thirteenth embodiment device manufactured by such a method [is] was evaluated [on the] as to its suitability immediately after forming [of] the lead wire portion 4, and [there are] no unsuitable (defective) lead wire portions were found at all in all the evaluated [ones] devices. When [the] an appearance inspection [is executed] was performed immediately after dicing, it [is] was found that there [are] were no defective semiconductor packages at all, and when the same temperature test as that performed for the first embodiment device [is executed] was carried out, it [is] was also found that there [are] were no defective samples at all.

[0103]

Fig. 14 is a cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a fourteenth embodiment of the present invention. Also, Fig. 40 is a view showing a semiconductor device according to a fourteenth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 14 shows a sectional view taken along lines A-B in Fig. 40.

[0104]

In Fig. 14 and Fig. 40, the same [numeral is] numerals are assigned to each of the same components as those shown in Fig. 11.

[0105]

The constituent difference between the aforementioned semiconductor device of the eleventh embodiment (hereinafter[, referred to as the eleventh embodiment device again) and the semiconductor device of the fourteenth embodiment (hereinafter[, referred to as the fourteenth embodiment device) is only [a point] that, with respect to the constitution of the slit portion of the stress cushioning layer 3, the slit portion of the semiconductor element protective layer 7[, and the slit portion of the conductor protective layer 5 on the end surface 1(1) of the semiconductor element 1, the eleventh embodiment device is structured so that the end face of the semiconductor element protective layer 7 and the end face of the stress cushioning layer 3 are [installed] disposed on the same plane and the end face of the conductor protective layer 5 is positioned [on the inside] inwardly compared with this same plane, while the fourteenth embodiment device is structured so that the end face of the semiconductor element protective layer 7 and the end face of the stress cushioning layer 3 are [installed] disposed on the same plane [and], while the end face of the conductor protective layer 5 is positioned [on the] outside [compared with] of this same plane [and] so that the outside part of the conductor protective layer 5 [of the outside part] reaches the end surface 1(1) [and there]. There are no other constituent differences between the eleventh embodiment device and the fourteenth embodiment device. Therefore, additional explanation [on] of the constitution of the fourteenth



embodiment device will be omitted.

[0106]

The [manufacturing] method of manufacture of the  
fourteenth embodiment device is the same as [the manufacturing  
5 method] that of the eleventh embodiment device, so that [the]  
an explanation [on] of the [manufacturing] method of  
manufacture of the fourteenth embodiment device will be  
omitted.

[0107]

10 The fourteenth embodiment device manufactured by such a  
method [is] was evaluated [on the] as to its suitability  
immediately after forming [of] the lead wire portion 4, and  
[there are] no unsuitable (defective) lead wire portions were  
found at all in all the evaluated [ones] devices. When [the]  
15 an appearance inspection [is executed] was performed  
immediately after dicing, it [is] was found that there [are]  
were no defective semiconductor packages at all, and when the  
same temperature test as that performed for the first  
embodiment device [is executed] was carried out, it [is] was  
20 also found that there [are] were no defective samples at all.

[0108]

Fig. 15 is a cross sectional view showing the  
constitution of [the essential] a typical section of the  
semiconductor device [of the] according to a fifteenth  
25 embodiment of the present invention. Also, Fig. 43 is a view  
showing a semiconductor device according to a fifteenth  
embodiment of this invention and illustrates the structure of

its substantial part. Further, Fig. 15 shows a sectional view taken along lines A-B in Fig. 43.

[0109]

In Fig. 15 and Fig. 43, the same [numeral is] are  
5 assigned to each of the same components as those shown in Fig. 12.

[0110]

The constituent difference between the aforementioned semiconductor device of the twelfth embodiment (hereinafter[,]  
10 referred to as the twelfth embodiment device again) and the semiconductor device of the fifteenth embodiment (hereinafter[,]  
referred to as the fifteenth embodiment device) is only [a point] that, with respect to the constitution of the slit portion of the stress cushioning  
15 layer 3 and the slit portion of the conductor protective layer 5 on the end surface 1(1) of the semiconductor element 1, the twelfth embodiment device is structured so that the end face of the conductor protective layer 5 is positioned [on the inside compared] inwardly with respect to the end face of the  
20 stress cushioning layer 3, while the fifteenth embodiment device is structured so that the end face of the conductor protective layer 5 is positioned on the outside compared with the end face of the stress cushioning layer 3 and the outside part of the conductor protective layer 5 [of the outside part]  
25 reaches the exposed end surface 7(2) of the semiconductor element protective layer 7 [and there]. There are no other constituent differences between the twelfth embodiment device

and the fifteenth embodiment device. Therefore, additional explanation [on] of the constitution of the fifteenth embodiment device will be omitted.

[0111]

5           The [manufacturing] method of manufacture of the fifteenth embodiment device is the same as [the manufacturing method] that of the twelfth embodiment device, so that the explanation [on] of the manufacturing method of the fifteenth embodiment device will be omitted.

10          [0112]

          The fifteenth embodiment device manufactured by such a method [is] was evaluated [on the] as to its suitability immediately after forming [of] the lead wire portion 4, and [there are] no unsuitable (defective) lead wire portions were found at all in all the evaluated [ones] devices. When [the] an appearance inspection [is ] was performed executed immediately after dicing, it [is] was found that there [are] were no defective semiconductor packages at all, and when the same temperature test as that performed for the first  
15          embodiment device [is executed] was carried out, it [is also] was found that there [are] were no defective samples at all.

[0113]

          Fig. 16 is a cross sectional view showing the constitution of [the essential] a typical section of the  
25          semiconductor device [of the] according to a sixteenth embodiment of the present invention. Also, Fig. 40 is a view showing a semiconductor device according to a sixteenth

embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 16 shows a sectional view taken along lines A-B in Fig. 40.

[0114]

5 In Fig. 16 and Fig. 40, the same [numeral is] numerals are assigned to each of the same components as those shown in Fig. 12.

[0115]

10 The constituent difference between the aforementioned semiconductor device of the twelfth embodiment (hereinafter[, referred to as the twelfth embodiment device again) and the semiconductor device of the sixteenth embodiment (hereinafter[, referred to as the sixteenth embodiment device) is only [a point] that, with respect to the

15 constitution of the slit portion of the semiconductor element protective layer 7, the slit portion of the stress cushioning layer 3[, and the slit portion of the conductor protective layer 5 on the end surface 1(1) of the semiconductor element 1, the twelfth embodiment device is structured so that the end

20 face of the conductor protective layer 5 is positioned [on the inside] inwardly compared with the end face of the stress cushioning layer 3, while the sixteenth embodiment device is structured so that the end face of the conductor protective layer 5 is positioned [on the] outside [as compared with] of

25 the end face of the stress cushioning layer 3, and the end face of the semiconductor element protective layer 7 and the outside part of the conductor protective layer 5 [of the

outside part] reaches the exposed end surface 7(2) of the semiconductor element protective layer 7 and the end surface 1(1) of the semiconductor element 1 [and there]. There are no other constituent differences between the twelfth embodiment device and the sixteenth embodiment device. Therefore, additional explanation [on] of the constitution of the sixteenth embodiment device will be omitted.

[0116]

The [manufacturing] method of manufacture of the sixteenth embodiment device is the same as [the manufacturing method] that of the twelfth embodiment device, so that [the] an explanation [on] of the [manufacturing] method of manufacture of the sixteenth embodiment device will be omitted.

[0117]

The sixteenth embodiment device manufactured by such a method [is] was evaluated [on the] as to its suitability immediately after forming [of] the lead wire portion 4, and [there are] no unsuitable (defective) lead wire portions were found at all in all the evaluated [ones] devices. When [the] an appearance inspection [is executed] was performed immediately after dicing, it [is] was found that there [are] were no defective semiconductor packages at all, and when the same temperature test as that performed for the first embodiment device [is executed] was carried out, it [is also] was found that there [are] were no defective samples at all.

[0118]

Fig. 17 is a cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a seventeenth embodiment of the present invention. Also, Fig. 40 is a view showing a semiconductor device according to a seventeenth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 17 shows a sectional view taken along lines A-B in Fig. 40.

[0119]

In Fig. 17 and Fig. 40, the same [numeral is] numerals are assigned to each of the same components as those shown in Fig. 13.

[0120]

The constituent difference between the aforementioned semiconductor device of the thirteenth embodiment (hereinafter[,] referred to as the thirteenth embodiment device again) and the semiconductor device of the seventeenth embodiment (hereinafter[,] referred to as the seventeenth embodiment device) is only [a point] that, with respect to the constitution of the slit portion of the stress cushioning layer 3 and the slit portion of the conductor protective layer 5 on the end surface 1(1) of the semiconductor element 1, the thirteenth embodiment device is structured so that the end face of the conductor protective layer 5 is positioned [on the inside] inwardly compared with the end face of the stress cushioning layer 3, while the seventeenth embodiment device is structured so that the end face of the conductor protective

layer 5 is positioned [on the] outside [compared with] of the end face of the stress cushioning layer 3, and the outside part of the conductor protective layer 5 [of the outside part] reaches the end surface 1(1) of the semiconductor element 1 [and there]. There are no other constituent differences between the thirteenth embodiment device and the seventeenth embodiment device. Therefore, additional explanation [on] of the constitution of the seventeenth embodiment device will be omitted.

[0121]

The [manufacturing] method of manufacture of the seventeenth embodiment device is the same as [the manufacturing method] that of the thirteenth embodiment device, so that [the] an explanation [on] of the [manufacturing] method of manufacture of the seventeenth embodiment device will be omitted.

[0122]

The seventeenth embodiment device manufactured by such a method [is] was evaluated [on the] as to its suitability immediately after forming [of] the lead wire portion 4, and [there are] no unsuitable (defective) lead wire portions were found at all in all the evaluated [ones] devices. When [the] an appearance inspection [is executed] was performed immediately after dicing, it [is] was found that there [are] were no defective semiconductor packages at all, and when the same temperature test as that performed for the first embodiment device [is executed] was carried out, it [is] was

also found that there [are] were no defective samples at all.  
[0123]

Fig. 18 is a cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to an eighteenth embodiment of the present invention. Also, Fig. 40 is a view showing a semiconductor device according to an eighteenth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 18 shows a sectional view taken along lines A-B in Fig. 40.

[0124]

In Fig. 18 and Fig. 40, the same [numeral is] numerals are assigned to each of the same components as those shown in Fig. 10.

[0125]

The constituent difference between the aforementioned semiconductor device of the tenth embodiment (hereinafter[, ] referred to as the tenth embodiment device again) and the semiconductor device of the eighteenth embodiment (hereinafter[, ] referred to as the eighteenth embodiment device) is only [a point] that, with respect to the constitution of the end area of the stress cushioning layer 3 and the end area of the conductor protective layer 5, the tenth embodiment device is structured so that a slit portion is formed in the stress cushioning layer 3, and a slit portion is also formed in the conductor protective layer 5, and their end faces are [installed] disposed on the same plane, while



the eighteenth embodiment device is structured so that a tapered portion becoming thinner [taperingly] toward the end face is formed on the stress cushioning layer 3, and a slit portion is formed in the conductor protective layer 5, [and] whereby the end (end face) of the tapered portion and the end face of the slit portion are [installed] disposed on the same plane, and the thickness of the conductor protective layer 5 [replenishes to] compensates for changes in the thickness of the tapered portion [and there]. There are no other constituent differences between the tenth embodiment device and the eighteenth embodiment device. Therefore, additional explanation [on] of the constitution of the eighteenth embodiment device will be omitted.

[0126]

As compared with the [manufacturing] method of manufacture of the tenth embodiment device, the [manufacturing] method of manufacture of the eighteenth embodiment device [has] is different only [a difference] in that, with respect to the [forming] means of forming the stress cushioning layer 3, the manufacturing method of the tenth embodiment device forms the stress cushioning layer 3 including the opening 3(1) having a gently-inclined rising portion using the mask printing method and then forms a slit portion in the stress cushioning layer 3 by laser processing, while the manufacturing method of the eighteenth embodiment device forms the stress cushioning layer 3 including the opening 3(1) having a gently-inclined rising portion and a

tapered portion becoming thinner [taperingly] toward the end face using the mask printing method and does not perform the subsequent laser processing for the stress cushioning layer 3 [and there]. There are no other differences between the manufacturing method of the tenth embodiment device and the manufacturing method of the eighteenth embodiment device. Therefore, additional explanation [on] of the manufacturing method of the eighteenth embodiment device will be omitted. [0127]

The eighteenth embodiment device manufactured by such a method [is] was evaluated [on the] as to its suitability immediately after forming [of] the lead wire portion 4, and [there are] no unsuitable (defective) lead wire portions were found at all in all the evaluated [ones] devices. When [the] an appearance inspection [is executed] was performed immediately after dicing, it [is] was found that there [are] were no defective semiconductor packages at all, and when the same temperature test as that performed for the first embodiment device [is executed] was carried out, it [is also] was found that there [are] were no defective samples at all. [0128]

Fig. 19 is a cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a nineteenth embodiment of the present invention. Also, Fig. 41 is a view showing a semiconductor device according to a nineteenth embodiment of this invention and illustrates the structure of

its substantial part. Further, Fig. 19 shows a sectional view taken along lines A-B in Fig. 41.

[0129]

In Fig. 19 and Fig. 41, the same [numeral is] numerals  
5 are assigned to each of the same components as those shown in Figs. 5 and 18.

[0130]

The constituent difference between the aforementioned semiconductor device of the eighteenth embodiment  
10 (hereinafter[,] referred to as the eighteenth embodiment device again) and the semiconductor device of the nineteenth embodiment (hereinafter[,] referred to as the nineteenth embodiment device) is only [a point] that, with respect to the constitution of the end (end face) of the stress cushioning  
15 layer 3 and the end (end face) of the conductor protective layer 5, the eighteenth embodiment device is structured so that the end (end face) of the stress cushioning layer 3 and the end face of the conductor protective layer 5 are  
[installed] disposed on the same plane, while the nineteenth  
20 embodiment device is structured so that the end (end face) of the conductor protective layer 5 is positioned [on the inside] inwardly compared with the end (end face) of the stress cushioning layer 3, and [the] an exposed end surface 3(2) is  
[installed] provided on the stress cushioning layer 3 [and  
25 there]. There are no other constituent differences between the eighteenth embodiment device and the nineteenth embodiment device. Therefore, additional explanation [on] of the

constitution of the nineteenth embodiment device will be omitted.

[0131]

5 The [manufacturing] method of manufacture of the nineteenth embodiment device is the same as [the manufacturing method] that of the eighteenth embodiment device except [a point] that the mask printing method is used for forming the conductor protective layer 5 [in stead] instead of the screen printing method[, so that the]. Thus, an explanation of the  
10 manufacturing method of the nineteenth embodiment device will be [also] omitted.

[0132]

The nineteenth embodiment device manufactured by such a method [is] was evaluated [on the] as to its suitability  
15 immediately after forming [of] the lead wire portion 4, and [there are] no unsuitable (defective) lead wire portions were found at all in all the evaluated [ones] devices. When [the] an appearance inspection [is executed] was performed immediately after dicing, it [is] was found that there [are]  
20 were no defective semiconductor packages at all, and when the same temperature test as that performed for the first embodiment device [is executed] was carried out, it [is also] was found that there [are] were no defective samples at all.

[0133]

25 Fig. 20 is a cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a twentieth

embodiment of the present invention. Also, Fig. 42 is a view showing a semiconductor device according to a twentieth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 20 shows a sectional view taken along lines A-B in Fig. 42.

[0134]

In Fig. 20 and Fig. 42, the same [numeral is] numerals are assigned to each of the same components as those shown in Figs. 12 and 19.

[0135]

The constituent difference between the aforementioned semiconductor device of the nineteenth embodiment (hereinafter[,] referred to as the nineteenth embodiment device again) and the semiconductor device of the twentieth embodiment (hereinafter[,] referred to as the twentieth embodiment device) is only [a point] that, with respect to the constitution of the end (end face) of the semiconductor element protective layer 7 and the end (end face) of the stress cushioning layer 3, the nineteenth embodiment device is structured so that the end face of the semiconductor element protective layer 7 and the end (end face) of the stress cushioning layer 3 are [installed] disposed on the same plane, while the twentieth embodiment device is structured so that the end face of the semiconductor element protective layer 7 is positioned [on the] outside [compared with] of the end (end face) of the stress cushioning layer 3 and [the] an exposed end surface 7(2) is [installed] provided on the semiconductor

element protective layer 7 [and there]. There are no other constituent differences between the nineteenth embodiment device and the twentieth embodiment device. Therefore, additional explanation [on] of the constitution of the  
5 twentieth embodiment device will be omitted.

[0136]

The [manufacturing] method of manufacture of the twentieth embodiment device is the same as [the manufacturing method] that of the nineteenth embodiment device except [a  
10 point] that the screen printing method is used for forming the conductor protective layer 5 [in stead] instead of the mask printing method[, so that the]. Thus, an explanation of the manufacturing method of the twentieth embodiment device will be [also] omitted.

15 [0137]

The twentieth embodiment device manufactured by such a method [is] was evaluated [on the] as to its suitability immediately after forming [of] the lead wire portion 4, and [there are] no unsuitable (defective) lead wire portions were  
20 found at all in all the evaluated [ones] devices. When [the] an appearance inspection [is executed] was performed immediately after dicing, it [is] was found that there [are] were no defective semiconductor packages at all, and when the same temperature test as that performed for the first  
25 embodiment device [is executed] was carried out, it [is also] was found that there [are] were no defective samples at all.

[0138]

Fig. 21 is a cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a twenty-first embodiment of the present invention. Also, Fig. 41 is a view showing a semiconductor device according to a twenty-first embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 21 shows a sectional view taken along lines A-B in Fig. 41.

[0139]

In Fig. 21 and Fig. 41, the same [numeral is] numerals are assigned to each of the same components as those shown in Fig. 19.

[0140]

The constituent difference between the aforementioned semiconductor device of the nineteenth embodiment (hereinafter[,] referred to as the nineteenth embodiment device again) and the semiconductor device of the twenty-first embodiment (hereinafter[,] referred to as the twenty-first embodiment device) is only [a point] that, with respect to the constitution of the end (end face) of the semiconductor element protective layer 7 and the end (end face) of the stress cushioning layer 3, the nineteenth embodiment device is structured so that the end face of the semiconductor element protective layer 7 and the end (end face) of the stress cushioning layer 3 are [installed] disposed on the same plane, while the twenty-first embodiment device is structured so that the end face of the semiconductor element protective layer 7

is positioned [on the inside compared with] inwardly relative  
to the end (end face) of the stress cushioning layer 3, [and]  
practically [installed] on the same plane as that of the end  
face of the conductor protective layer 5 [and there]. There  
5 are no other constituent differences between the nineteenth  
embodiment device and the twenty-first embodiment device.  
Therefore, additional explanation [on] of the constitution of  
the twenty-first embodiment device will be omitted.

[0141]

10 The [manufacturing] method of manufacture of the twenty-  
first embodiment device is the same as [the manufacturing  
method] that of the nineteenth embodiment device, so that  
[the] an explanation [on] of the [manufacturing] method of  
manufacture of the twenty-first embodiment device will be  
15 omitted.

[0142]

The twenty-first embodiment device manufactured by such a  
method [is] was evaluated [on the] as to its suitability  
immediately after forming [of] the lead wire portion 4, and  
20 [there are] no unsuitable (defective) lead wire portions were  
found at all in all the evaluated [ones] devices. When [the]  
an appearance inspection [is executed] was performed  
immediately after dicing, it [is] was found that there [are]  
were no defective semiconductor packages at all, and when the  
25 same temperature test as that performed for the first  
embodiment device [is executed] was carried out, it [is also]  
was found that there [are] were no defective samples at all.



[0143]

Fig. 22 is a cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a twenty-second embodiment of the present invention. Also, Fig. 40 is a view showing a semiconductor device according to a twenty-second embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 22 shows a sectional view taken along lines A-B in Fig. 40.

[0144]

In Fig. 22 and Fig. 40, the same [numeral is] numerals are assigned to each of the same components as those shown in Fig. 18.

[0145]

The constituent difference between the aforementioned semiconductor device of the eighteenth embodiment (hereinafter[,] referred to as the eighteenth embodiment device again) and the semiconductor device of the twenty-second embodiment (hereinafter[,] referred to as the twenty-second embodiment device) is only [a point] that, with respect to the constitution of the end area of the conductor protective layer 5, the eighteenth embodiment device is structured so that a slit portion is formed in the conductor protective layer 5 and the end face of the conductor protective layer 5 is almost perpendicular to the end surface 1(1), while the twenty-second embodiment device is structured so that an inclined surface becoming thinner linearly toward

the end face of the conductor protective layer 5 is formed  
[and there]. There are no other constituent differences  
between the eighteenth embodiment device and the twenty-second  
embodiment device. Therefore, additional explanation [on] of  
5 the constitution of the twenty-second embodiment device will  
be omitted.

[0146]

When the [manufacturing] method of manufacture of the  
twenty-second embodiment device is compared with [the  
10 manufacturing method] that of the eighteenth embodiment  
device, the difference is only [a point] that, with respect to  
the [forming] means of forming the conductor protective player  
5, the manufacturing method of the eighteenth embodiment  
device forms the conductor protective layer 5 including the  
15 opening 3(1) having a gently-inclined rising portion and a  
slit portion having an end face almost perpendicular to the  
end surface 1(1) using the screen printing method, while the  
manufacturing method of the twenty-second embodiment device  
forms the conductor protective layer 5 including the opening  
20 3(1) having a gently-inclined rising portion and an inclined  
surface having a linearly-inclined rising portion using the  
screen printing method [and there]. There are no other  
differences between the manufacturing method of the eighteenth  
embodiment device and the manufacturing method of the twenty-  
25 second embodiment device. Therefore, additional explanation  
[on] of the manufacturing method of the twenty-second  
embodiment device will be omitted.

[0147]

The twenty-second embodiment device manufactured by such a method [is] was evaluated [on the] as to its suitability immediately after forming [of] the lead wire portion 4, and [there are] no unsuitable (defective) lead wire portions were found at all in all the evaluated [ones] devices. When [the] an appearance inspection [is executed] was performed immediately after dicing, it [is] was found that there [are] were no defective semiconductor packages at all, and when the same temperature test as that performed for the first embodiment device [is executed] was carried out, it [is also] was found that there [are] were no defective samples at all.

[0148]

Fig. 23 is a cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a twenty-third embodiment of the present invention. Also, Fig. 41 is a view showing a semiconductor device according to a twenty-third embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 23 shows a sectional view taken along lines A-B in Fig. 41.

[0149]

In Fig. 23 and Fig. 41, the same [numeral is] numerals are assigned to each of the same components as those shown in Figs. 5 and 22.

[0150]

The constituent difference between the aforementioned

semiconductor device of the twenty-second embodiment

(hereinafter[,] referred to as the twenty-second embodiment device again) and the semiconductor device of the twenty-third embodiment (hereinafter[,] referred to as the twenty-third

5 embodiment device) is only [a point] that, with respect to the constitution of the end (end face) of the stress cushioning

layer 3 and the end (end face) of the conductor protective layer 5, the twenty-second embodiment device is structured so that the end (end face) of the stress cushioning layer 3 and

10 the end (end face) of the conductor protective layer 5 are [installed] disposed on the same plane, while the twenty-third embodiment device is structured so that the end (end face) of the conductor protective layer 5 is positioned [on the inside compared with] inwardly relative to the end (end face) of the

15 stress cushioning layer 3, and [the] an exposed end surface 3(2) is [installed] provided on the stress cushioning layer 3 [and there]. There are no other constituent differences

between the twenty-second embodiment device and the twenty-third embodiment device. Therefore, additional explanation

20 [on] of the constitution of the twenty-third embodiment device will be omitted.

[0151]

The [manufacturing] method of manufacture of the twenty-third embodiment device is the same as the manufacturing

25 [method] that of the twenty-second embodiment device except [a point] that the mask printing method is used for forming the conductor protective layer 5 [in stead] instead of the screen

printing method[, so that the]. Thus, an explanation of the manufacturing method of the twenty-third embodiment device will be [also] omitted.

[0152]

5           The twenty-third embodiment device manufactured by such a method [is] was evaluated [on the] as to its suitability immediately after forming [of] the lead wire portion 4, and [there are] no unsuitable (defective) lead wire portions were found at all in all the evaluated [ones] devices. When [the] 10 an appearance inspection [is executed] was performed immediately after dicing, it [is] was found that there [are] were no defective semiconductor packages at all, and when the same temperature test as that performed for the first embodiment device [is executed] was carried out, it [is also] 15 was found that there [are] were no defective samples at all.  
[0153]

          Fig. 24 is a cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a twenty-fourth 20 embodiment of the present invention. Also, Fig. 42 is a view showing a semiconductor device according to a twenty-fourth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 24 shows a sectional view taken along lines A-B in Fig. 42.  
25   [0154]

          In Fig. 24 and Fig. 42, the same [numeral is] numerals are assigned to each of the same components as those shown in

Figs. 20 and 23.

[0155]

The constituent difference between the aforementioned semiconductor device of the twenty-third embodiment (hereinafter[,] referred to as the twenty-third embodiment device again) and the semiconductor device of the twenty-fourth embodiment (hereinafter[,] referred to as the twenty-fourth embodiment device) is only [a point] that, with respect to the constitution of the end face of the semiconductor element protective layer 7 and the end (end face) of the stress cushioning layer 3, the twenty-third embodiment device is structured so that the end face of the semiconductor element protective layer 7 and the end (end face) of the stress cushioning layer 3 are [installed] disposed on the same plane, while the twenty-fourth embodiment device is structured so that the end face of the semiconductor element protective layer 7 is positioned [on the] outside [compared with] of the end (end face) of the stress cushioning layer 3, and [the] an exposed end surface 7(2) is [installed] provided on the semiconductor element protective layer 7 [and there]. There are no other constituent differences between the twenty-third embodiment device and the twenty-fourth embodiment device. Therefore, additional explanation [on] of the constitution of the twenty-fourth embodiment device will be omitted.

[0156]

The [manufacturing] method of manufacture of the twenty-fourth embodiment device is the same as [the manufacturing

method] that of the twenty-third embodiment device, except [a point] that the screen printing method is used for forming the conductor protective layer 5 [in stead] instead of the mask printing method[, so that the]. Thus, an explanation of the manufacturing method of the twenty-fourth embodiment device will be [also] omitted.

[0157]

The twenty-fourth embodiment device manufactured by such a method [is] was evaluated [on the] as to its suitability immediately after forming [of] the lead wire portion 4, and [there are] no unsuitable (defective) lead wire portions found at all in all the evaluated [ones] devices. When [the] an appearance inspection [is executed] was performed immediately after dicing, it [is] was found that there [are] were no defective semiconductor packages at all, and when the same temperature test as that performed for the first embodiment device [is executed] was carried out, it [is also] was found that there [are] were no defective samples at all.

[0158]

Fig. 25 is a cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a twenty-fifth embodiment of the present invention. Also, Fig. 41 is a view showing a semiconductor device according to a twenty-fifth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 25 shows a sectional view taken along lines A-B in Fig. 41.

[0159]

In Fig. 25 and Fig. 41, the same [numeral is] numerals are assigned to each of the same components as those shown in Fig. 23.

5 [0160]

The constituent difference between the aforementioned semiconductor device of the twenty-third embodiment (hereinafter[,] referred to as the twenty-third embodiment device again) and the semiconductor device of the twenty-fifth embodiment (hereinafter[,] referred to as the twenty-fifth embodiment device) is only [a point] that, with respect to the constitution of the end (end face) of the semiconductor element protective layer 7 and the end (end face) of the stress cushioning layer 3, the twenty-third embodiment device is structured so that the end face of the semiconductor element protective layer 7 and the end (end face) of the stress cushioning layer 3 are [installed] disposed on the same plane, while the twenty-fifth embodiment device is structured so that the end face of the semiconductor element protective layer 7 is positioned [on the inside compared with] inwardly of the end (end face) of the stress cushioning layer 3, [and] practically [installed] on the same plane as that of the end (end face) of the conductor protective layer 5 [and there]. There are no other constituent differences between the twenty-third embodiment device and the twenty-fifth embodiment device. Therefore, additional explanation [on] of the constitution of the twenty-fifth embodiment device will be

10  
15  
20  
25



omitted.

[0161]

The [manufacturing] method of manufacture of the twenty-fifth embodiment device is the same as [the manufacturing method] that of the twenty-third embodiment device, so that [the] an explanation on the [manufacturing] method of manufacture of the twenty-fifth embodiment device will be [also] omitted.

[0162]

The twenty-fifth embodiment device manufactured by such a method [is] was evaluated [on the] as to its suitability immediately after forming [of] the lead wire portion 4, and [there are] no unsuitable (defective) lead wire portions were found at all in all the evaluated [ones] devices. When [the] an appearance inspection [is executed] was performed immediately after dicing, it [is] was found that there [are] were no defective semiconductor packages at all, and when the same temperature test as that performed for the first embodiment device [is executed] was carried out, it [is also] was found that there [are] were no defective samples at all.

[0163]

Fig. 26 is a cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a twenty-sixth embodiment of the present invention. Also, Fig. 40 is a view showing a semiconductor device according to a twenty-sixth embodiment of this invention and illustrates the structure of

its substantial part. Further, Fig. 26 shows a sectional view taken along lines A-B in Fig. 40.

[0164]

In Fig. 26 and Fig. 40, the same [numeral is] numerals  
5 are assigned to each of the same components as those shown in Fig. 18.

[0165]

The constituent difference between the aforementioned semiconductor device of the eighteenth embodiment  
10 (hereinafter[,] referred to as the eighteenth embodiment device again) and the semiconductor device of the twenty-sixth embodiment (hereinafter[,] referred to as the twenty-sixth embodiment device) is only [a point] that, with respect to the constitution of the end face of the semiconductor element  
15 protective layer 7, the end (end face) of the stress cushioning layer 3[,] and the end face of the conductor protective layer 5, the eighteenth embodiment device is structured so that the end face of the semiconductor element protective layer 7, the end (end face) of the stress  
20 cushioning layer 3, and the end face of the conductor protective layer 5 are [installed] disposed on the same plane, while the twenty-sixth embodiment device is structured so that, although the end face of the semiconductor element protective layer 7 and the end (end face) of the stress  
25 cushioning layer 3 are positioned on the same plane, the end face of the semiconductor element protective layer 7 is positioned [on the] outside [compared with the same] of this

plane, and the outside part of the semiconductor element protective layer 7 [of the outside part] reaches the end surface 1(1) of the semiconductor element 1[, and there].

There are no other constituent differences between the  
5 eighteenth embodiment device and the twenty-sixth embodiment device. Therefore, additional explanation [on] of the constitution of the twenty-sixth embodiment device will be omitted.

[0166]

10 The [manufacturing] method of manufacture of the twenty-sixth embodiment device is the same as [the manufacturing method] that of the eighteenth embodiment device[, so that the]. Thus, an explanation [on] of the manufacturing method of the twenty-sixth embodiment device will be [also] omitted.

15 [0167]

The twenty-sixth embodiment device manufactured by such a method [is] was evaluated [on the] as to its suitability immediately after forming [of] the lead wire portion 4, and [there are] no unsuitable (defective) lead wire portions were  
20 found at all in all the evaluated [ones] devices. When [the] an appearance inspection [is executed] was performed immediately after dicing, it [is] was found that there [are] were no defective semiconductor packages at all, and when the same temperature test as that performed for the first  
25 embodiment device [is executed] was carried out, it [is also] was found that there [are] were no defective samples at all.

[0168]

Fig. 27 is a cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a twenty-seventh embodiment of the present invention. Also, Fig. 43 is a view showing a semiconductor device according to a twenty-seventh embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 27 shows a sectional view taken along lines A-B in Fig. 43.

[0169]

In Fig. 27 and Fig. 43, the same [numeral is] numerals are assigned to each of the same components as those shown in Fig. 20.

[0170]

The constituent difference between the aforementioned semiconductor device of the twentieth embodiment (hereinafter[,] referred to as the twentieth embodiment device again) and the semiconductor device of the twenty-seventh embodiment (hereinafter[,] referred to as the twenty-seventh embodiment device) is only [a point] that, with respect to the constitution of the end face of the conductor protective layer 5, the twentieth embodiment device is structured so that the end face of the conductor protective layer 5 is positioned [on the inside compared with] inwardly of the end face of the stress cushioning layer 3, while the twenty-seventh embodiment device is structured so that the end face of the conductor protective layer 5 is positioned [on the] outside [compared with] of the end face of the stress cushioning layer 3, and

the outside part of the conductor protective layer 5 of the outside part reaches the exposed end surface 7(2) of the semiconductor element protective layer 7 [and there]. There are no other constituent differences between the twentieth embodiment device and the twenty-seventh embodiment device. Therefore, additional explanation [on] of the constitution of the twenty-seventh embodiment device will be omitted.

[0171]

The [manufacturing] method of manufacture of the twenty-seventh embodiment device is the same as [the manufacturing method] that of the twentieth embodiment device except [a point] that the mask printing method is used for forming the conductor protective layer 5 [in stead] instead of the screen printing method[, so that the]. Thus, an explanation of the manufacturing method of the twenty-seventh embodiment device will be [also] omitted.

[0172]

The twenty-seventh embodiment device manufactured by such a method [is] was evaluated [on the] as to its suitability immediately after forming [of] the lead wire portion 4, and [there are] no unsuitable (defective) lead wire portions were found at all in all the evaluated [ones] devices. When [the] an appearance inspection [is executed] was performed immediately after dicing, it [is] was found that there [are] were no defective semiconductor packages at all, and when the same temperature test as that performed for the first embodiment device [is executed] was carried out, it [is also]

was found that there [are] were no defective samples at all.

[0173]

Fig. 28 is a cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a twenty-eighth embodiment of the present invention. Also, Fig. 40 is a view showing a semiconductor device according to a twenty-eighth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 28 shows a sectional view taken along lines A-B in Fig. 40.

[0174]

In Fig. 28 and Fig. 40, the same [numeral is] numerals are assigned to each of the same components as those shown in Fig. 27.

[0175]

The constituent difference between the aforementioned semiconductor device of the twenty-seventh embodiment (hereinafter[,] referred to as the twenty-seventh embodiment device again) and the semiconductor device of the twenty-eighth embodiment (hereinafter[,] referred to as the twenty-eighth embodiment device) is only [a point] that, with respect to the constitution of the end face of the conductor protective layer 5, the twenty-seventh embodiment device is structured so that the end face of the conductor protective layer 5 is positioned [on the inside compared with] inwardly of the end face of semiconductor element protective layer 7 and on the outside compared with the end (end face) of the

stress cushioning layer 3, while the twenty-eighth embodiment device is structured so that the end face of the conductor protective layer 5 is positioned on the outside compared with the end face of the semiconductor element protective layer 7 and the end (end face) of the stress cushioning layer 3 [and there]. There are no other constituent differences between the twenty-seventh embodiment device and the twenty-eighth embodiment device. Therefore, additional explanation [on] of the constitution of the twenty-eighth embodiment device will be omitted.

[0176]

The [manufacturing] method of manufacture of the twenty-eighth embodiment device is the same as [the manufacturing method] that of the twenty-seventh embodiment device except [a point] that the screen printing method is used for forming the conductor protective layer 5 [in stead] instead of the mask printing method[, so that the]. Thus, an explanation of the manufacturing method of the twenty-eighth embodiment device will be [also] omitted.

[0177]

The twenty-eighth embodiment device manufactured by such a method [is] was evaluated [on the] as to its suitability immediately after forming [of] the lead wire portion 4, and [there are] no unsuitable (defective) lead wire portions were found at all in all the evaluated [ones] devices. When [the] an appearance inspection [is executed] was performed immediately after dicing, it [is] was found that there [are]

were no defective semiconductor packages at all, and when the same temperature test as that performed for the first embodiment device [is executed] was carried out, it [is also] was found that there [are] were no defective samples at all.

5 [0178]

Fig. 29 is a cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a twenty-ninth embodiment of the present invention. Also, Fig. 40 is a view  
10 showing a semiconductor device according to a twenty-ninth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 29 shows a sectional view taken along lines A-B in Fig. 40.

[0179]

15 In Fig. 29 and Fig. 40, the same [numeral is] numerals are assigned to each of the same components as those shown in Fig. 28.

[0180]

The constituent difference between the aforementioned  
20 semiconductor device of the twenty-eighth embodiment (hereinafter[, ] referred to as the twenty-eighth embodiment device again) and the semiconductor device of the twenty-ninth embodiment (hereinafter[, ] referred to as the twenty-ninth embodiment device) is only [a point] that, with respect to the  
25 constitution of the end face of the conductor protective layer 5 and the end (end face) of the stress cushioning layer 3, the twenty-eighth embodiment device is structured so that the end



(end face) of the stress cushioning layer 3 is positioned [on the] inside [compared with] of the end face of the semiconductor element protective layer 7, while the twenty-ninth embodiment device is structured so that the end (end face) of the stress cushioning layer 3 is positioned [on the] outside [compared with] of the end face of the semiconductor element layer 7, and the end (end face) of the stress cushioning layer 3 [of the outside part] reaches the surface of the semiconductor element 1 [and there]. There are no other constituent differences between the twenty-eighth embodiment device and the twenty-ninth embodiment device. Therefore, additional explanation [on] of the constitution of the twenty-ninth embodiment device will be omitted.

[0181]

The [manufacturing] method of manufacture of the twenty-ninth embodiment device is the same as [the manufacturing method] that of the twenty-eighth embodiment device, except [a point] that the mask printing method is used for forming the conductor protective layer 5 [in stead] instead of the screen printing method[, so that the]. Thus, an explanation of the manufacturing method of the twenty-ninth embodiment device will be [also] omitted.

[0182]

The twenty-ninth embodiment device manufactured by such a method [is] was evaluated [on the] as to its suitability immediately after forming [of] the lead wire portion 4, and [there are] no unsuitable (defective) lead wire portions were

found at all in all the evaluated [ones] devices. When [the] an appearance inspection [is executed] was performed immediately after dicing, it [is] was found that there [are] were no defective semiconductor packages at all, and when the same temperature test as that performed for the first embodiment device [is executed] was carried out, it [is also] was found that there [are] were no defective samples at all.  
[0183]

Fig. 30 is a cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a thirtieth embodiment of the present invention. Also, Fig. 40 is a view showing a semiconductor device according to a thirtieth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 30 shows a sectional view taken along lines A-B in Fig. 40.  
[0184]

In Fig. 30 and Fig. 40, the same [numeral is] numerals are assigned to each of the same components as those shown in Fig. 22.  
[0185]

The constituent difference between the aforementioned semiconductor device of the twenty-second embodiment (hereinafter[,] referred to as the twenty-second embodiment device again) and the semiconductor device of the thirtieth embodiment (hereinafter[,] referred to as the thirtieth embodiment device) is only [a point] that, with respect to the

constitution of the end face of the conductor protective layer 5, the twenty-second embodiment device is structured so that the end face of the semiconductor element protective layer 7, the end (end face) of the stress cushioning layer 3[,] and the end (end face) of the conductor protective layer 5 are [respectively installed] disposed on the same plane, while the thirtieth embodiment device is structured so that the end face of the semiconductor element protective layer 7 and the end (end face) of the stress cushioning layer 3 are [installed] disposed on the same plane, [and] while the end (end face) of the conductor protective layer 5 is positioned [on the] outside compared with this same plane, and the end (end face) of the conductor protective layer 5 [of the outside part] reaches the surface of the semiconductor element 1 [and there]. There are no other constituent differences between the twenty-second embodiment device and the thirtieth embodiment device. Therefore, additional explanation [on] of the constitution of the thirtieth embodiment device will be omitted.

[0186]

The [manufacturing] method of manufacture of the thirtieth embodiment device is the same as [the manufacturing method] that of the twenty-second embodiment device[, so that the]. Thus, an explanation [on] of the manufacturing method of the thirtieth embodiment device will be [also] omitted.

[0187]

The thirtieth embodiment device manufactured by such a

method [is] was evaluated [on the] as to its suitability immediately after forming [of] the lead wire portion 4, and [there are] no unsuitable (defective) lead wire portions were found at all in all the evaluated [ones] devices. When [the] an appearance inspection [is executed] was performed immediately after dicing, it [is] was found that there [are] were no defective semiconductor packages at all, and when the same temperature test as that performed for the first embodiment device [is executed] was carried out, it [is also] was found that there [are] were no defective samples at all.

[0188]

Fig. 31 is a cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a thirty-first embodiment of the present invention. Also, Fig. 42 is a view showing a semiconductor device according to a thirty-first embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 31 shows a sectional view taken along lines A-B in Fig. 42.

[0189]

In Fig. 31 and Fig. 42, the same [numeral is] numerals are assigned to each of the same components as those shown in Fig. 24.

[0190]

The constituent difference between the aforementioned semiconductor device of the twenty-fourth embodiment (hereinafter[,] referred to as the twenty-fourth embodiment

device again) and the semiconductor device of the thirty-first embodiment (hereinafter[,] referred to as the thirty-first embodiment device) is only [a point] that, with respect to the constitution of the end (end face) of the stress cushioning layer 3 and the end (end face) of the conductor protective layer 5, the twenty-fourth embodiment device is structured so that the end (end face) of the stress cushioning layer 3 is positioned [on the] outside [compared with] of the end (end face) of the conductor protective layer 5 and [the] an exposed end surface 3(2) is [installed] provided on the stress cushioning layer 3, while the thirty-first embodiment device is structured so that the end face of the semiconductor element protective layer 7 and the end (end face) of the stress cushioning layer 3 are [installed] disposed on the same plane and the end (end face) of the stress cushioning layer 3 is positioned [on the] inside [compared with] of the end (end face) of the conductor protective layer 5 [and there]. There are no other constituent differences between the twenty-fourth embodiment device and the thirty-first embodiment device. Therefore, additional explanation [on] of the constitution of the thirty-first embodiment device will be omitted.

[0191]

The [manufacturing] method of manufacture of the thirty-first embodiment device is the same as [the manufacturing method] that of the twenty-fourth embodiment device except [a point] that the mask printing method is used for forming the conductor protective layer 5 [in stead] instead of the screen

printing method[, so that the]. Thus, an explanation of the manufacturing method of the thirty-first embodiment device will be [also] omitted.

[0192]

5           The thirty-first embodiment device manufactured by such a method [is] was evaluated [on the] as to its suitability immediately after forming [of] the lead wire portion 4, and [there are] no unsuitable (defective) lead wire portions were found at all in all the evaluated [ones] devices. When [the] 10 an appearance inspection [is executed] was performed immediately after dicing, it [is] was found that there [are] were no defective semiconductor packages at all, and when the same temperature test as that performed for the first embodiment device [is executed] was carried out, it [is also] 15 was found that there [are] were no defective samples at all.  
[0193]

Fig. 32 is a cross sectional view showing the constitution of [the essential] a typical section of the semiconductor device [of the] according to a thirty-second 20 embodiment of the present invention. Also, Fig. 40 is a view showing a semiconductor device according to a thirty-second embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 32 shows a sectional view taken along lines A-B in Fig. 40.

25           [0194]

In Fig. 32 and Fig. 40, the same [numeral is] numerals are assigned to each of the same components as those shown in

Fig. 28.

[0195]

The constituent difference between the aforementioned semiconductor device of the twenty-eighth embodiment (hereinafter[, referred to as the twenty-eighth embodiment device again) and the semiconductor device of the thirty-second embodiment (hereinafter[, referred to as the thirty-second embodiment device) is only [a point] that, with respect to the constitution of the end (end face) of the conductor protective layer 5, the twenty-eighth embodiment device is structured so that the end face of the conductor protective layer 5 is installed on the surface of the semiconductor element 1 [in the standing state] and is vertical thereto due to [forming] formation of the slit portion, while the thirty-second embodiment device is structured so that the end (end face) of the conductor protective layer 5 is formed as a plurality of inclined surfaces having a different inclination angle stepwise [and there]. There are no other constituent differences between the twenty-eighth embodiment device and the thirty-second embodiment device. Therefore, additional explanation [on] of the constitution of the thirty-second embodiment device will be omitted.

[0196]

The [manufacturing] method of manufacture of the thirty-second embodiment device is the same as [the manufacturing method] that of the twenty-eighth embodiment device[, so that the]. Thus, an explanation [on] of the manufacturing method

of the thirty-second embodiment device will be [also] omitted.  
[0197]

The thirty-second embodiment device manufactured by such  
a method [is] was evaluated [on the] as to its suitability  
5 immediately after forming [of] the lead wire portion 4<sub>L</sub> and  
[there are] no unsuitable (defective) lead wire portions were  
found at all in all the evaluated [ones] devices. When [the]  
an appearance inspection [is executed] was performed  
immediately after dicing, it [is] was found that there [are]  
10 were no defective semiconductor packages at all<sub>L</sub> and when the  
same temperature test as that performed for the first  
embodiment device [is executed] was carried out, it [is also]  
was found that there [are] were no defective samples at all.  
[0198]

15 Fig. 33 is a cross sectional view showing the  
constitution of [the essential] a typical section of the  
semiconductor device [of the] according to a thirty-third  
embodiment of the present invention. Also, Fig. 40 is a view  
showing a semiconductor device according to a thirty-second  
20 embodiment of this invention and illustrates the structure of  
its substantial part. Further, Fig. 32 shows a sectional view  
taken along lines A-B in Fig. 40.  
[0199]

In Fig. 33 and Fig. 40, the same [numeral is] numerals  
25 are assigned to each of the same components as those shown in  
Fig. 29.  
[0200]



The constituent difference between the aforementioned semiconductor device of the twenty-ninth embodiment (hereinafter[, referred to as the twenty-ninth embodiment device again) and the semiconductor device of the thirty-third embodiment (hereinafter[, referred to as the thirty-third embodiment device) is only [a point] that, with respect to the constitution of the end (end face) of the conductor protective layer 5, the twenty-ninth embodiment device is structured so that the end face of the conductor protective layer 5 is [installed] disposed on the surface of the semiconductor element 1 [in the standing state] and is vertical thereto due to [forming] formation of the slit portion, while the thirty-third embodiment device is structured so that the end (end face) of the conductor protective layer 5 is formed as a plurality of inclined surfaces having a different inclination angle stepwise [and there]. There are no other constituent differences between the twenty-ninth embodiment device and the thirty-third embodiment device. Therefore, additional explanation [on] of the constitution of the thirty-third embodiment device will be omitted.

[0201]

The [manufacturing] method of manufacture of the thirty-third embodiment device is the same as [the manufacturing method] that of the twenty-ninth embodiment device[, so that the]. Thus, an explanation [on] of the manufacturing method of the thirty-third embodiment device will be [also] omitted.

[0202]

The thirty-third embodiment device manufactured by such a method [is] was evaluated [on the] as to its suitability immediately after forming [of] the lead wire portion 4, and [there are] no unsuitable (defective) lead wire portions ere found at all in all the evaluated [ones] devices. When [the] an appearance inspection [is executed] was performed immediately after dicing, it [is] was found that there [are] were no defective semiconductor packages at all, and when the same temperature test as that performed for the first embodiment device [is executed] was carried out, it [is also] was found that there [are] were no defective samples at all.  
[0203]

Meanwhile, with respect to the semiconductor element protective layer 7 to be used for the semiconductor [devicees] devices of the tenth to thirty-third embodiments, [if a usable] any material that can protect the semiconductor element 1 from [an] the external environment can be used, [it] so that the invention is not limited to use of the aforementioned negative type photosensitive polyimide resin. Namely, [the usable] materials that may be used are polyimide, polycarbonate, polyester, polytetrafluoroethylene, polyethylene, polypropylene, polyvinylidene fluoride, cellulose acetate, polysulfone, polyacrylonitrile, polyamide, polyamide-imide, epoxy, maleic-imide, phenol, cyanate, polyolefin, and polyurethane, compounds thereof, and mixtures of those compounds, and rubber components, such as acrylic rubber, silicone rubber, or nitrile-butadiene rubber, or an

organic compound filler, such as polyimide filler, or inorganic filler such as silica. Furthermore, photosensitive materials including these materials [may be used].

[0204]

5           With respect to the stress cushioning layer 3 to be used for the semiconductor devices of the first to thirty-third embodiments, [a usable] the material to be used is preferably a low-elastomeric resin because it must cushion stress. [Concretely, the usable] More specifically, materials that may  
10 be used are fluororubber, silicone rubber, silicone fluoride rubber, acrylic rubber, hydrogenated nitrile rubber, ethylene propylene rubber, chlorosulfonated polystyrene, epichlorohydrin rubber, butyl rubber, urethane rubber, polycarbonate/acrylonitrile butadiene styrene alloy,  
15 polysiloxane dimethyl terephthalate/polyethylene terephthalate copolymer polybutylene terephthalate/polycarbonate alloy, polytetrafluoroethylene, fluorinated ethylene propylene, polyarylate, polyamide/acrylonitrile butadiene styrene alloy, denatured epoxy, denatured polyolefin, and siloxane denatured  
20 polyamide-imide. In addition to them, various kinds of thermoset resins, or materials combining two or more thermoset resins, or materials with inorganic fillers mixed in thermoset resins may be used, such as epoxy resin, unsaturated polyester resin, epoxy isocyanate resin, maleic-imide resin, maleic-  
25 imide epoxy resin, cyanate ester resin, cyanate ester epoxy resin, cyanate ester maleic-imide resin, phenolic resin, diallyl phthalate resin, urethane resin, cyanamide resin, and

maleic-imide cyanamide resin. Further, if photosensitivity is given to these resins, [and] the form of the stress cushioning layer 3 can be controlled by a predetermined exposure-development process.

5 [0205]

In this case, with respect to the semiconductor device of the present invention, various kinds of semiconductor [devicees are] devices can be manufactured by changing the thickness of the stress cushioning layer 3 and the size of the semiconductor element 1, and each of the semiconductor [devicees is] devices can be mounted on a mounting substrate[, and the]. A mounting reliability evaluation test [is] was executed within the temperature range from -55°C to 125°C. The result of the test shows that, assuming the thickness of the stress cushioning layer 3 as t and the distance from the center of gravity of the semiconductor element 1 to the outermost end of the semiconductor element 1 as R, when the relationship of t and R satisfies the formula  $t/R \leq 0.01[.]$ , the mounting reliability is satisfactory.

20 [0206]

Furthermore, the lead wire portion 4 to be used for the semiconductor [devicees] devices of the first to thirty-third embodiments uses a material of gold (Au), copper (Cu), or aluminum (Al) or a material of copper (Cu) or aluminum (Al) with its surface plated with gold (Au).

25 [0207]

The conductor protective layer 5 to be used for the

semiconductor [devicees] devices of the first to thirty-third  
embodiments is not limited to the material [to be used]  
specified above. However, an organic combined part, such as  
epoxy resin, polyimide resin, or polyamide resin compounded  
5 with an inorganic filler, is generally formed on the stress  
cushioning layer 3, including the lead wire portion 4 and  
excluding the connected portion of the lead wire portion 4 and  
the external electrode 6 by screen printing. In this case, a  
material with a given photosensitivity [given] may be added.

10 [0208]

Furthermore, the external electrode 6 to be used for the  
semiconductor [devicees] devices of the first to thirty-third  
embodiments is a conductor electrically connected to the  
substrate with the semiconductor device mounted thereon, so  
15 that the material to be used may be[, concretely,] a solder  
alloy including tin (Sn), zinc (Zn), or lead (Pb), or silver  
(Ag), Copper (Cu), or gold (Au), or a solder alloy, silver  
(Ag), or copper (Cu) which is covered with gold (Au) and  
formed in a ball shape. In addition to these materials, a  
20 metal such as molybdenum (Mo), nickel (Ni), copper (Cu),  
platinum (Pt), or titanium (Ti), or an alloy composed of two  
or more kinds of the aforementioned metals, or a multi-layer  
composed of two or more layers may be used.

[0209]

25 Next, to compare differences in characteristics with the  
semiconductor [devicees] devices of the first to thirty-third  
embodiments, some semiconductor [devicees are] devices were

separately formed as comparison examples.

[0210]

Fig. 34 is a cross sectional view showing the constitution of [the essential] a typical section of a semiconductor device [as] representing a first comparison example. Also, Fig. 44 is a view showing a semiconductor device which is a first comparison example and illustrates the structure of its substantial part. Further, Fig. 34 shows a sectional view taken along lines A-B in Fig. 44.

[0211]

In Fig. 34 and Fig. 44, the same [numeral is] numerals are assigned to each of the same components as those shown in Fig. 1.

[0212]

The constituent difference between the aforementioned semiconductor device of the first embodiment (hereinafter[, referred to as the first embodiment device again) and the semiconductor device of the first comparison example (hereinafter[, referred to as the first comparison example device) is only [a point] that, with respect to the constitution of the end areas of the stress cushioning layer 3 and the conductor protective layer 5, the first embodiment device is structured so that the stress cushioning layer 3 and the conductor protective layer 5 have slit portions [reaching the bottom of] extending through the stress cushioning layer 3 and the [bottom of the] conductor protective layer 5, respectively, [thereby] so that the end face of the stress

cushioning layer 3 and the end face of the conductor protective layer 5 on the end surface 1(1) of the semiconductor element 1 are formed inside the cutting scribe line formed on a semiconductor wafer, and the end surface 1(1) of the semiconductor element 1 is exposed within the range from the end face to the inside of the scribe line[, while].On the other hand, the first comparison example device is structured so that the end face of the stress cushioning layer 3 and the end face of the conductor protective layer 5 are [installed] disposed on the same plane as that of the end face of the semiconductor element 1 and the semiconductor element 1 has no exposed end surface 1(1) [and there]. There are no other constituent differences between the first embodiment device and the first comparison example device. Therefore, additional explanation [on] of the constitution of the first comparison example device will be omitted.

[0213]

The [manufacturing] method of manufacture of this first comparison example device will be described hereunder.

Firstly, positioning marks made of aluminum (Al) indicating an intersection of scribe lines [are] were formed on one side of a semiconductor wafer of silicon (Si); and, in the areas enclosed by the positioning marks, the electrode pads 2 made of aluminum (Al) [are] were formed, respectively, and an integrated circuit portion (not shown in the drawing) [is] are formed.

[0214]

Next, on the one side of the semiconductor wafer [with]  
on which the positioning marks and electrode pads 2 are  
formed, an uncured dry film composed of epoxy resin,  
orthocresol novolac curing agent, acrylic rubber, and silica  
5 filler [which has], having a thickness of 100  $\mu\text{m}$  and a  
coefficient of elasticity of 3000 MPa at room temperature  
after curing, [is] was adhered in an environment of 150°C  
using a roll laminator, and the adhered dry film [is] was  
heated and cured at 150°C for one hour, thus the stress  
10 cushioning layer 3 [is] was formed.

[0215]

Next, [the] oxygen plasma etching [is executed] was  
carried out, and the residue of the stress cushioning layer 3  
on the electrode pads 2 [is] was removed[, and the]. The  
15 oxide film on the surface of the electrode pads 2 [is] was  
also removed, and then a chromium (Cr) film with a thickness  
of 500 Å [is] was deposited in the opening 3(1) of the stress  
cushioning layer 3 and on the stress cushioning layer 3  
[respectively, and a] itself. A copper (Cu) film with a  
20 thickness of 0.5  $\mu\text{m}$  [is] was then deposited on it. Then, a  
negative type photosensitive resist [is] was spin-coated on  
the deposited film and [then] prebaked, exposed, and  
developed, and a resist wiring pattern with a thickness of 15  
 $\mu\text{m}$  [is] was formed. A copper (Cu) film with a thickness of 10  
25  $\mu\text{m}$  [is] was formed inside the formed wiring pattern by  
electroplating, and a nickel (Ni) film with a thickness of 2  
 $\mu\text{m}$  [is] was formed on it by electroplating. Thereafter, the



resist [is] was peeled off [by] using a release liquid, and the copper (Cu) film in the deposited film [is] was etched by an ammonium persulfate/sulfuric acid solution[, and furthermore]. Furthermore, the chromium (Cr) film in the deposited film [is] was etched by a potassium permanganate solution, and the lead wire portion 4 [is] was formed. At the point of time when the lead wire portion 4 is formed, the same evaluation (the first evaluation) as that for the semiconductor device of the first embodiment [is] was performed.

[0216]

Then, a photosensitive solder resist varnish [is] was coated on the stress cushioning layer 3 including the lead wire portion 4 by screen printing, and the coated film [is] was dried at 80°C for 20 minutes, then exposed and developed using a predetermined pattern, and heated and cured at 150°C for one hour, [thereby] whereby the conductor protective layer 5 having a plurality of windows 5(1) at a part of the lead wire portion 4 [is] was formed.

[0217]

Next, a gold (Au) deposit film with a thickness of 0.1  $\mu\text{m}$  [is] was formed on the nickel (Ni) film of the lead wire portion 4, which is exposed via the windows 5(1) by replacement plating. Thereafter, flux [is] was coated on the gold (Au) deposit film using a metal mask, and solder balls of Sn-Ag-Cu series with a diameter of about 0.35 mm [are] were put on it, and the solder balls [are] were heated in an

infrared reflow furnace at 260°C for 10 seconds, [and] whereby  
the external electrodes 6 [are] were formed.

[0218]

Finally, the semiconductor chip [is] was cut with a  
5 dicing saw with a thickness of 0.2 mm along the scribe line  
and a plurality of semiconductor [devicees are] devices were  
obtained. In this case, the same evaluation (the second  
evaluation) as that for the semiconductor device of the first  
embodiment [is] was performed for the obtained semiconductor  
10 [devicees] devices, and moreover, the same temperature test as  
that for the semiconductor device of the first embodiment [is  
executed] was carried out, and then the evaluation ([the] a  
third evaluation) [is] was performed again.

[0219]

15 In the semiconductor [devicees] devices of the first  
comparison example manufactured by such a manufacturing  
method, at the first evaluation time, defective conductor  
patterns of about 30% [are] were generated for the lead wire  
portion 4, and at the second evaluation (appearance  
20 inspection) time immediately after dicing, defective  
semiconductor [devicees] devices of about 20% [are] were  
generated because large mechanical stress [is] was applied to  
the cutting portion of a plurality of layers during dicing[,  
and furthermore]. Furthermore, at the third evaluation time  
25 after the temperature test, package defects, such as a  
disconnection defect, [are] were generated in almost all  
samples because large mechanical stress during dicing and also

large thermal stress during the changing of the temperature  
[are] were applied to the cutting portion of a plurality of  
layers.

[0220]

5           Fig. 35 is a cross sectional view showing the  
constitution of [the essential] a typical section of a  
semiconductor device [as] representing a second comparison  
example. Also, Fig. 44 is a view showing a semiconductor  
device which is a second comparison example and illustrates  
10   the structure of its substantial part. Further, Fig. 35 shows  
a sectional view taken along lines A-B in Fig. 44.

[0221]

          In Fig. 35 and Fig. 44, the same [numeral is] numerals  
are assigned to each of the same components as those shown in  
15   Fig. 6.

[0222]

          The constituent difference between the aforementioned  
semiconductor device of the sixth embodiment (hereinafter[,]  
referred to as the sixth embodiment device again) and the  
20   semiconductor device of the second comparison example  
(hereinafter[,] referred to as the second comparison example  
device) is only [a point] that, with respect to the  
constitution of the end area of the stress cushioning layer 3,  
the sixth embodiment device is structured so that the  
25   conductor protective layer 5 has a slit portion reaching the  
bottom thereof, [thereby] so that the end face of the  
conductor protective layer 5 on the end surface 1(1) of the

semiconductor element 1 is formed inside the cutting scribe line formed on a semiconductor wafer, and the end surface 1(1) of the semiconductor element 1 is exposed within the range from the end face to the inside of the scribe line, while the second comparison example device is structured so that the end face of the conductor protective layer 5 is installed on the same plane as that of the end face of the semiconductor element 1 and the semiconductor element 1 has no exposed end surface 1(1) [and there]. There are no other constituent differences between the sixth embodiment device and the second comparison example device. Therefore, additional explanation [on] of the constitution of the second comparison example device will be omitted.

[0223]

As compared with the [manufacturing] method of manufacture of the sixth embodiment device, the [manufacturing] method of manufacturing of the second comparison example device [has] is different only [a difference] in that, in the [manufacturing method] manufacture of the sixth embodiment device, [forms] a slit portion is formed in the conductor protective layer 5 when the conductor protective layer 5 is formed by screen printing, while the [manufacturing] method of manufacture of the second comparison example device forms no slit in the conductor protective layer 5 [and there]. There are no other differences between the manufacturing method of the sixth embodiment device and the manufacturing method of the second comparison example device.

Therefore, additional explanation [on] of the manufacturing method of the second comparison example device will be omitted.

[0224]

5           In the semiconductor [devicees] devices of the second comparison example manufactured by such a manufacturing method, at the first evaluation time, defective conductor patterns of 30% or more [are] were generated for the lead wire portion 4, and at the second evaluation (appearance  
10 inspection) time immediately after dicing, defective semiconductor [devicees] devices of about 20% [are] were generated during dicing[, and furthermore]. Furthermore, at the third evaluation time, after the temperature test, package defects, such as a disconnection defect, [are] were generated  
15 in almost all samples.

[0225]

Fig. 36 is a cross sectional view showing the constitution of [the essential] a typical section of a semiconductor device [as] representing a third comparison  
20 example. Also, Fig. 44 is a view showing a semiconductor device which is a third comparison example and illustrates the structure of its substantial part. Further, Fig. 36 shows a sectional view taken along lines A-B in Fig. 44.

[0226]

25           In Fig. 36 and Fig. 44, the same [numeral is] numerals are assigned to each of the same components as those shown in Fig. 10.

[0227]

The constituent difference between the aforementioned semiconductor device of the tenth embodiment (hereinafter[, referred to as the tenth embodiment device again) and the semiconductor device of the third comparison example (hereinafter[, referred to as the third comparison example device) is only [a point] that, with respect to the constitution of the respective end areas of the semiconductor element protective layer 7, the stress cushioning layer 3[, and the conductor protective layer 5, the tenth embodiment device is structured so that the semiconductor element protective layer 7, the stress cushioning layer 3[, and the conductor protective layer 5 [respectively] have slit portions reaching the bottom of the semiconductor element protective layer 7, the bottom of the stress cushioning layer 3, and the bottom of the conductor protective layer 5, [thereby] so that the end face of the semiconductor element protective layer 7, the end face of the stress cushioning layer 3, and the end face of the conductor protective layer 5 on the end surface 1(1) of the semiconductor element 1 are formed inside the cutting scribe line formed on a semiconductor wafer, and the end surface 1(1) of the semiconductor element 1 is exposed within the range from the end face to the inside of the scribe line[, while]. On the other hand, the third comparison example device is structured so that the end face of the semiconductor element protective layer 7, the end face of the stress cushioning layer 3, and the end face of the conductor

protective layer 5 are respectively installed on the same plane as that of the end face of the semiconductor element 1 and the semiconductor element 1 has no exposed end surface 1(1) [and there]. There are no other constituent differences between the tenth embodiment device and the third comparison example device. Therefore, additional explanation [on] of the constitution of the third comparison example device will be omitted.

[0228]

The [manufacturing] method of manufacture of the third comparison example device is the same as the [manufacturing] method of manufacture of the tenth embodiment device, so that the explanation on the manufacturing method of the third comparison example device will be omitted.

[0229]

In the semiconductor [devicees] devices of the third comparison example manufactured by such a manufacturing method, at the first evaluation time, defective conductor patterns of slightly lower than 30% [are] were generated for the lead wire portion 4, and at the second evaluation (appearance inspection) time, immediately after dicing, defective semiconductor [devicees] devices of about 30% [are] were generated during dicing[, and furthermore]. Furthermore, at the third evaluation time, after the temperature test, package defects such as a disconnection defect, [are] were generated in almost all samples.

[0230]

Fig. 37 is a cross sectional view showing the constitution of [the essential] a typical section of a semiconductor device [as] representing a fourth comparison example. Also, Fig. 44 is a view showing a semiconductor device which is a forth comparison example and illustrates the structure of its substantial part. Further, Fig. 37 shows a sectional view taken along lines A-B in Fig. 44.

[0231]

In Fig. 37 and Fig. 44, the same [numeral is] numerals are assigned to each of the same components as those shown in Fig. 28.

[0232]

The constituent difference between the aforementioned semiconductor device of the twenty-eighth embodiment (hereinafter[,] referred to as the twenty-eighth embodiment device again) and the semiconductor device of the fourth comparison example (hereinafter[,] referred to as the fourth comparison example device) is only [a point] that, with respect to the constitution of the respective end areas of the semiconductor element protective layer 7 and the conductor protective layer 5, the twenty-eighth embodiment device is structured so that the semiconductor element protective layer 7 and the conductor protective layer 5 respectively have slit portions reaching the bottom of the semiconductor element protective layer 7 and the bottom of the conductor protective layer 5, [thereby] so that the end face of the conductor protective layer 5 is positioned on the outside compared with



the end face of the semiconductor element protective layer 7,  
and the end face of the conductor protective layer 5 is formed  
inside the cutting scribe line formed on a semiconductor  
wafer, [and] whereby the end surface 1(1) of the semiconductor  
5 element 1 is exposed within the range from the end face to the  
inside of the scribe line[, while]. On the other hand, the  
fourth comparison example device is structured so that the end  
face of the semiconductor element protective layer 7 and the  
end face of the conductor protective layer 5 are respectively  
10 installed on the same plane as that of the end face of the  
semiconductor element 1, and the semiconductor element 1 has  
no exposed end surface 1(1) [and there]. There are no other  
constituent differences between the twenty-eighth embodiment  
device and the fourth comparison example device. Therefore,  
15 additional explanation [on] of the constitution of the fourth  
comparison example device will be omitted.

[0233]

The [manufacturing] method of manufacture of the fourth  
comparison example device is the same as the [manufacturing]  
20 method of manufacture of the twenty-eighth embodiment device,  
so that the explanation [on] of the manufacturing method of  
the fourth comparison example device will be omitted.

[0234]

In the semiconductor [devicees] devices of the fourth  
25 comparison example manufactured by such a manufacturing  
method, at the first evaluation time, defective conductor  
patterns of about 30% [are] were generated for the lead wire

portion 4, and at the second evaluation (appearance inspection) time, immediately after dicing, defective semiconductor [devicees] devices of about 30% [are] were generated during dicing[, and furthermore]. Furthermore, at the third evaluation time, after the temperature test, package defects, such as a disconnection defect, [are] were generated in almost all samples.

[0235]

As mentioned above, as compared with the semiconductor [devicees] devices of the first to fourth comparison examples, the semiconductor [devicees] devices of the first to thirty-third embodiments are structured so that the respective end faces of the stress cushioning layer 3 and the conductor protective layer 5, or the respective end faces of the semiconductor element protective layer 7, the stress cushioning layer 3, and the conductor protective layer 5, are formed inside the scribe line inside the end face of the semiconductor element 1, so that a semiconductor wafer can be cut by surely recognizing the positioning marks [put] located on the semiconductor wafer during cutting of the semiconductor wafer, [and] whereby occurrences of defective semiconductor packages due to variations of the cutting position of each of the obtained semiconductor devicees can be eliminated.

[0236]

In the semiconductor [devicees] devices of the first to thirty-third embodiments, when each semiconductor device is to be obtained by cutting a semiconductor wafer, the cut portion

of each semiconductor device is formed as a single-layer structure of only [a] the semiconductor [elementso], so that even if mechanical stress is generated during cutting of the semiconductor wafer, the mechanical stress is just applied to the single-layer structure and a plurality of resin layers can be prevented from peeling off due to the mechanical force.

[0237]

Furthermore, in the semiconductor [devicees] devices of the first to thirty-third embodiments, even if thermal stress is generated due to great changes in the environmental temperature during mounting of each semiconductor device and the thermal stress is applied to a plurality of resin layers, large mechanical stress is not applied to the plurality of resin layers during cutting of [a] the semiconductor wafer and the plurality of resin layers are little damaged, so that peeling-off of the plurality of resin layers due to the thermal stress does not occur at all or very little.

[0238]

#### [Effects of the Invention]

As mentioned above, according to the semiconductor device and semiconductor device manufacturing method of the present invention, the respective end faces of the stress cushioning layer and conductor protective layer, or the respective end faces of the semiconductor element protective layer, stress cushioning layer, and conductor protective layer in the end surface area of the semiconductor element, are formed inside the semiconductor wafer cutting scribe line, and the

semiconductor element is exposed within the range from the end face to the inside of the scribe line, so that when the semiconductor wafer is to be cut along the semiconductor wafer cutting scribe line, it can be cut by surely recognizing the positioning marks [put] located on the semiconductor wafer and an effect can be produced such that occurrences of defective semiconductor packages due to variations in the cutting position of each obtained semiconductor device can be eliminated.

[0239]

According to the semiconductor device and semiconductor device manufacturing method of the present invention, when each semiconductor device is to be obtained by cutting a semiconductor wafer, the cut portion of each semiconductor device is formed as a single-layer structure of only [a] semiconductor element, and even if mechanical stress is generated during cutting of the semiconductor wafer, the mechanical stress is just applied to the single-layer structure, so that an effect can be produced such that a plurality of resin layers will not be peeled off by the mechanical force.

[0240]

Furthermore, according to the semiconductor device and semiconductor device manufacturing method of the present invention, even if thermal stress is generated due to great changes in the environmental temperature during mounting of each semiconductor device and the thermal stress is applied to

a plurality of resin layers, large mechanical stress is not applied to the plurality of resin layers during cutting of [a] the semiconductor wafer, and the plurality of resin layers are little damaged, so that an effect can be produced such that the plurality of resin layers will not be peeled off [not] at all or very little by the thermal stress.

[0241]

As a result, according to the semiconductor device and semiconductor device manufacturing method of the present invention, an effect can be produced such that each semiconductor device is not damaged [not] at all or very little by application of mechanical stress and thermal stress thereto, [and] whereby the reliability of semiconductor [devicees] devices can be enhanced, and the yield rate during [manufacturing] manufacture of semiconductor [devicees] devices can be improved.

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8. A semiconductor device according to Claim 6 or 7,  
wherein said end face of said semiconductor element  
protective player is formed outside said end face of  
5 said stress cushioning layer.

9. A semiconductor device according to Claim 6 or 7,  
wherein said end face of said semiconductor element  
protective player is formed inside said end face of  
10 said stress cushioning layer.

10. A semiconductor device according to any of Claims  
4 to <sup>7</sup>9, wherein an end area of said stress cushioning  
layer is formed so as to become taperingly thinner  
15 toward the said end face.

11. A semiconductor device manufacturing method  
comprising a first step of forming a plurality of  
semiconductor elements having an integrated circuit  
20 and an electrode pad on a circuit forming surface of a  
semiconductor wafer, a second step of forming a stress  
cushioning layer on a plurality of semiconductor  
elements, a third step of forming an opening in an  
electrode pad of said stress cushioning layer and  
25 forming a notch wider than a width of a scribe line in

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## ABSTRACT OF THE DISCLOSURE

The present invention is <sup>A</sup>a semiconductor device  
 having <sup>a</sup>the semiconductor element <sup>is</sup> obtained by cutting  
 a semiconductor wafer <sup>, having an</sup> with the electrode pad [2] formed  
 on one side <sup>thereof,</sup> along <sup>a</sup>the scribe line [1]. The semiconductor <sup>device has a</sup> semiconductor  
 element protective layer [7] on the semiconductor  
 element [1] which has <sup>so as to form an</sup> the opening [7(1)] <sup>above</sup> on the pad [2], <sup>a</sup>the  
 stress cushioning layer [3] on the layer [7] which has <sup>so as to form an</sup> the  
 opening [3(1)] on the pad [2], <sup>a</sup>the lead wire portion [4]  
 reaching the layer [3] from the electrode pad [2] via the  
 openings [7(1)] and [3(1)], <sup>a</sup>the external electrodes [6] on  
 the lead wire portion [4] and <sup>a</sup>the conductor protective  
 layer [5] on the layer [3] and <sup>a</sup>the layer [7], the layer [3],  
 and the conductor protective layer [5] form <sup>a</sup>the  
 respective end faces on the end surface [1(1)] of the  
 semiconductor element [1] inside the scribe line and  
 expose <sup>a surface of the semiconductor element</sup> the range from the end face of the end surface  
 [1(1)] <sup>a point</sup> to <sup>, thereby to expose the scribe line</sup> the inside of the scribe line.